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Evolution of Maskless Digital Lithography: Game-changer for Advanced Semiconductor Packaging

Abstract: *Lithography is a fundamental process in semiconductor chip manufacturing, patterning the chip design onto the photoresist coated wafer substrate before it is further processed for creating the device architectures. At one end, cutting EUV lithography is shaping the 3-5nm devices with masks and advanced OPC (optical proximity correction algorithms), and at the other end, newer maskless lithography technologies are shaping patterning at 2micron (predicted to touch 500nm) for other emerging applications in micro-electronics with new commercial propositions and actualization TAT. This paper gives a comparative overview of these patterning technologies and their potent applications in the semiconductor industry.*

Keywords: *Lithography, semiconductor patterning, maskless lithography, digital lithography*

I. INTRODUCTION

Lithography is a fundamental manufacturing process in semiconductor chip fabs for transferring the chip design to a substrate. Traditionally, commercial semiconductor industry is dominated by high-throughput lithography systems that image the circuit pattern on a substrate coated with a photoresist. Patterning a circuit is a primary first process step in the electronics industry from PCB to the high precision engineered semiconductor dies in a semiconductor fab facility to the creation of flat panel display circuity on a large glass substrate in a display fab facility.

With the industry evolution to advanced semiconductor packaging and multi-geometry die integration in a package, the backend-of-line manufacturing processes are replicating frontend-of-line processes. This evolution is scaling high volume manufacturing of advanced packages by mass processing of dies on a base substrate (wafer-or panel-level packaging) which coated with polymers and then RDLs (redistribution layers) route the die outputs to the real-world.

Traditional solutions like lithographic tools are now getting challenged by a new genre of patterning technology, vis, maskless digital lithography which saves on interim process steps that add to both the process cost and turn-around-time.

This paper gives an overview of the patterning technologies and brings out the opportunity that the new maskless digital technology delivers to the semiconductor packaging industry.

II. CURRENT PATTERNING APPROACHES

At the heart of each patterning approach is the exposure unit that defines the characteristic performance of that specific lithographic technique (Abdelhanin, 2017). The different image patterning systems in the market can be classified into four broad categories based on the exposure methods they use:

A. Mask based Contact and Proximity Proximity Printing Systems

Mask-based contact printers use a system assembly/platform for aligning and holding the target substrate in a firm, physical contact with the mask. Next. the mask is exposed to high-intensity,

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collimated laser beam (at wavelengths as per photo-resist sensitivity). This transfers the mask pattern on to the target.

1. Mask based contact and proximity printing systems,
2. Mask (reticle)-based projection systems (conventional, step-and-repeat, and scanning),
3. Focused-beam direct-writing systems, and
4. Maskless Digital Lithography.

A summary of these techniques is shared in table 1 and each of these is briefly described here.

B. Mask-based Projection Systems

Mask-based contact printers use a system assembly/platform for aligning and holding the target substrate in a firm, physical contact with the mask.

Next. the mask is exposed to high-intensity, collimated laser beam (at wavelengths as per photo-resist sensitivity). This transfers the mask pattern on to the target.

On the other hand, proximity systems maintain a precise, fixed gap between the mask and the target. Typically, such systems use one/ two mercury arc lamps, with power ratings in range of 2-8 kW. The photoresist is exposed to UV radiation in the range ˜250 nm to ˜430 nm - the rest of the lamp radiation in the infrared and the visible range is filtered thru appropriate traps to minimize substrate heating. Such lamp sources have very poor energy utilization & the useful UV energy is barely 1% of the lamp wattage.

Repeated contact between mask and the resist-coated surface leads to a range of defects on the substrate and this is a major limitation of contact printing. It also results in poor yields. Repeated contact of a mask with substrates also progressively lowers the mask life and increases the overall effective costs of such a system. While these issues are relatively subdued in proximity printing, there the feature size is impacted by proximity variations between mask & substrate.

If mask-substrate gap is ‘d’ for a proximity printer using a wavelength λ, its resolution R is given by $R = (\lambda\ d/2)^2$.

Table 1. Overview of Exposure Techniques for Image Patterning

S. No	Exposure Method	Contact/Proximity Printing Systems	Reticle-based Projection Steppers	Focused Beam Direct Imaging	Maskless Digital Lithography
1.	Exposure Field Size	Full Field	Reticle-size limited (up to 50mm x 25mm)	Individual beam spots (Laser)	Clustered write heads (using Digital Micromirror Devices (DMD))
2.	Exposure Wavelength/ Beam Optics	Broadband (g, h, i-line)/ Top Hat Beam	i-line/ broadband Top Hat beam	Single wavelength Gaussian or Top Hat beam	Multiple-wavelength exposure optics Top Hat Beam
3.	Resolution L/S	>3 µm	>1.5 µm	Can do 600nm at very restricted throughput	< 2 µm
4.					

Source: Adapted from Industry notes

As is evident, resolution is quite sensitive to d and this limitation increases with large target substrates (example: flat panel displays in a display fab) as it becomes difficult to maintain a consistent, precise gap d between the mask and the target. The target is further subject to warpage and there can be surface deformities from wafer to wafer. These realities are just some of the limitations of the mask-based systems discussed further as well.

C. Mask-based Projection Systems

For fabrication of microelectronic modules, patterning can be achieved using a wide variety of image projection systems. In the simplest image projection system, image (field) at the lens is patterned on the entire target substrate. These are called single-step (or single-field) tools and are the most conventional/ simplest projection systems that typically use a projection lens with a 1:1 (zero gain) magnification. To increase the targeted resolution, the lithographic system will produce a smaller image on the target substrate. In the single step conventional projection patterning systems, there is a trade-off between the target substrate size and the desired resolution for the image pattern.

Step-and-repeat projection systems pattern the image again and again in steps across the target substrate which is divided into several segments. Each segment is imaged one at a time by stepping the substrate under the lens from one segment to the next segment. Step-and-repeat patterning process will deliver lower throughputs as there is an additional overhead time for the stepping, and precisely aligning steps for each segment. Typical step-and-repeat systems use reduction patterning, with a 2:1, 5:1 or 10:1 ratio. For higher resolution, systems with larger reduction ratios are used. This is at the expense of lower throughput as more steps are required to cover the target area. Stitching errors between adjacent exposure segments are common performance issues in step-and-repeat projection systems. In a step-and-repeat patterning system in semiconductor chip lithography, each die segment is separated by scribe lanes through which the chips are diced. In a typical litho patterning process, the mask (reticle) needs to precisely step-and-repeat imaged for delivering a well-articulated pattern. Stitching errors in lithography can dramatically reduce yield and play with factory ROI in real life. Over the last 2 decades, several scanning projection tools have been developed to address the throughput limitations of step-and-repeat projection patterning systems. Scanning ring-field imaging patterning systems will use primary imaging mirrors that are approximately three times the size of the substrate. While the use of larger optics improves the overall resolution, these solutions can be quite expensive. Moreover, such patterning systems cannot be reliably created in practice for large panel lithography applications. Throughput is another issue with these systems.

Yet another class of scanning systems use an adapted Dyson-type imaging system with a large beam splitter, a reduction ratio of 4:1, and separate mask and substrate platform stages with precisely controlled motion. While these systems can improve the resolution 250 nanometers, they will have die-field-size limitations (of~ 7 cm^2). Moreover, precision engineering in such systems, tight IP control and market dynamics have driven capital costs for such systems to the range of ~ $10+ million and current lead-times for supply of such systems run into years.

Masks for projection lithography systems – called ‘reticles’ in industry parlance- are significantly less vulnerable to damage than masks used in contact and proximity printers. However, the use of a ‘physical’ mask in the patterning process brings in limitations on the production efficiency.

A reliable, high-throughput lithography system is critical to the commercial fabrication of microelectronic components like integrated circuits (small format packages featuring dies of ~1sq cm size or lesser), printed circuit boards (typical area patterned could be a few sq inches) or flat panel displays (large-area patterning on substrates of sizes ~30-40 sq ft). Reliable throughput determines the yield - and is a critical determinant of the economic success or failure of a semiconductor fabrication facility. For high-volume manufacturing, optical lithography has emerged as the defact commercial technology as it can achieve high throughput because it can pattern a complete image simultaneously (in parallel) and not thru a sequential imaging. In optical lithography several features are printed in parallel onto a target in a single exposure that illuminates a mask to transfer its pattern onto the target. Size and

complexity of the circuit pattern shape the size and complexity of the corresponding reticle (mask) that is used for the patterning. Using an appropriate mask optical lithography can precisely and efficiently pattern a circuit irrespective of its size and complexity.

Despite the obvious benefits of parallel processing, several factors can significantly impact the efficiency and speed performance of the optical lithography process. For example, 'baking' a pattern on a substrate will be a function of photoresist sensitivity and that will also be a function of the intensity of the illumination and the specific wavelength of the illuminating beam. - the exposure speed can be improved by using a photo resist with higher sensitivity and an illuminating beam of higher intensity for the right wavelength. Complex circuits, with many layers of features, will require additional process steps and exposures by switching of masks. Each layer is patterned layer by layer – for each layer the reticle (mask) has to be positioned and aligned with precision before then exposure is done. In this switching of masks and repositioning, the throughput falls and adds to the costs. Additionally, the semiconductor fab maintains an inventory of masks to process various circuits that it fabricates. The masks are precision engineered, have a lead time of supply – and are not available off-the-shelf. Moreover, mask (reticle) makers are in huge demand and facility may also decide to have a backup inventory. Mask-based patterning therefore has inherently higher cost of purchasing and maintaining this inventory overhead.

A common problem with masks in optical lithography is procuring and maintaining them. Masks are procured from outsourced specialist organizations and it is typically a suppliers' market. Typical turnaround times for arranging a prototype mask will run into months. Moreover, prototype mask development is an iterative process in real life – and the prototype mask may be used briefly and then replaced as the prototype is refined. Such operating costs as well delays in prototype turn-around times are real and can become quite significant with trial and retrials with numerous masks in the prototyping process.

Moreover, as the size of the mask increases, its cost scales up. Flat Panel display prototype development, with need for large-area masks for multiple iterations of prototyping, can be a very costly proposition.

Mask-based patterning enables high volume manufacturing in lithography with parallel processing, but at significantly higher costs and TAT exposures. Mask-based patterning limits the manufacturing process by adding the process time overhead for switching and aligning masks - and the costs of maintaining inventories of masks.

Imagine the benefits if need to change masks manually in-situ during the production process was eliminated and if the parallel processing power of a mask were maintained. This would significantly reduce the manufacturing time overhead. Imagine if the need for inventories of production masks was eliminated. This would dramatically reduce the manufacturing overhead costs of these inventories. In a process where masks were eliminated, but a parallel exposure process kept intact, prototype development could proceed efficiently, with speed and economically. Such a mask-less patterning technology would enable a significant improvement in the productivity and process costs of the semiconductor, display and PCB fabrication industry.

D. Focused-beam Direct-writing System

Laser direct imaging technology is a possible solution to eliminating mask-related costs. However, direct imaging techniques involve sequential patterning as the laser beam writes point-by-point at significantly low throughput.

Functionally, the focused-beam direct-writing system uses a laser to sequentially raster scan the target substrate to create the pattern, pixel-by-pixel, on the target. Typically, laser light source can be Argon-ion based (using its UV or blue wavelengths) for maintaining compatibility with the spectral sensitivity of the popular photoresists. The laser beam is targeted on the photoresist-coated substrate to the appropriate gaussian or top-hat spot size. This collimated beam is stepped across the substrate in a raster scan (along the x-axis, say) driven by a high-precision stepping motor-driven mirror. Separately, the y-axis is enabled at the end of the x-axis scan, by another high-precision stepping motor that drives the platform holding the target substrate in an orthogonal direction. Simultaneously, the laser beam is modulated either in intensity or in frequency – and

can be even turned ‘on’ a pattern location on the target substrate or deflected away. With a rigorous algorithm that combines the beam modulation and the x-axis and y-axis stepper motors with appropriate pattern data, the complete target is patterned (albeit sequentially). There are several focused-beam direct-write systems available in the market and find usage in labs for R&DE/ prototyping work. Such systems have resolution that varies from few microns for printed-circuit board patterning to a fraction of micron for systems designed for applications for IC lithography. However, the patterning process is slow and not amenable to high-volume manufacturing. If the pattern is complex and the user desires a high-resolution image, the size of the file will be very high. Since the image is patterned by a sequential beam, pixel-by-pixel, the system can take anything from a couple of minutes to several hours per sq. ft. of pattern area. While the Direct write systems do not use physical masks, having replaced them with algorithm-driven beams— their significantly lower thruput limits their usage to R&DE labs.

E. Maskless Digital Lithography

Maskless Digital lithography techniques address the low thruput of a spot-focused direct writing system by using a reflective spatial light modulator to do a large-area, seamless patterning. Such reflective spatial light modulators are commercially realized in a Digital Micromirror Device (DMD). A DMD is now a well-tested, highly reliable microprocessor innovation that consists of an array of micro-scale mirror assemblies, each being settable to an “on” reflective angle as directly addressed by a controlling algorithm. A DMD can reflect a complete pattern – not just a pixel spot- via an optical projection system onto a photoresist-coated target substrate.

DMD is a commercially successful product from Texas Instrument. It is basically a highly reliable MEMS device with over the 2+ decades of proven performance in its innovation history.

The Digital Micromirror Device (DMD) is a MEMS-based opto-mechanical system that consists of an array of hinged micro-scale mirror assemblies. Each of the micromirrors can tilt into one of the two precisely controlled orientations. Its operation is primarily reflective. When a micromirror tilts in one orientation, it reflects the incident light beam through an optical imaging system which harvests the beam pattern by using it on a target substrate (and this harvest condition is referred to as ‘on’). A micromirror that tilts in the other orientation reflects the incident illumination away from the optical system; such a micromirror is referred to as ‘off.’ In typical implementations, the light reflected from the ‘off’ pixels are lost as it is not harvested unlike the ‘on’ system pattern. A DMD chip is conceptually created by depositing a reflective aluminum coating on a base substrate which will eventually be scribed into a rectangular array of several hundred thousand microscopic mirrors corresponding to the pixels in the image to be patterned. The mirrors and supporting mechanical structures are constructed in a MEMS fab using typical semiconductor microstructure creation processes. The array of micromirrors may be independently turned ‘on’ or ‘off’ and can be configured to form any desired pattern of ‘on’ elements, literally imaging a circuit pattern. When light falls on the DMD chip, it is reflected from the ‘on’ features and imaged by the optical system onto a target substrate. When the substrate is prepared with an appropriate photoresist, the image will have been patterned on the substrate and this is effectively replicating the mask based conventional lithography, albeit without a physical mask. Thus, in this maskless system, the DMD coupled with an imaging system replaces the mask-based conventional lithography systems.

It supports all commercially available resists and achieves similar patterning performance.

It is emerging as a powerful complement to other litho tools in the evolving semiconductor packaging process by offering advantages in cost of operations (CoO), TAT, and Scalability.

III. TECHNOLOGIES SHAPING MASKLESS DIGITAL LITHOGRAPHY

A. DMD

In a typical Maskless Digital Lithography tool, the DMD is a TI Digital Light Processor Chip (DLP) which acts as the ‘write head’ or ‘mask’ that takes the pattern from the image file and reproduces it through beam optics onto a substrate (Texas Instruments, USA, 2023) (Abdelhanin, 2017). The micro-mirrors are aluminum reflectors that are mounted on a base of MEMS-controlled hinges.

Over the last 2 decades of existence, DLP have established a high reliability history and are powering

a range of applications from consumer projectors to industrial tools (Douglas, 2003). It currently offers a 2000nm x 2000 nm resolution, and in the future, this could evolve to a 500 nm x 500 nm resolution.

B. Beam Optics

The light source directs a top hat beam on the DLP, and the DLP 'on' mirror converts it into a patterned light source that is focused onto the substrate kept on the exposure platform. DLP 'off' mirror light is dumped.

Top Hat beam ensures that there is a uniform light beam exposure on the DLP. This is also factored into the energy dose being delivered onto the photoresist-coated substrate via an optical system that can further reduce the image by a magnitude of order onto the substrate.

The combination of the laser source, the DMD, and the optical system is the 'Eye' of the Digital Litho tool.

C. Exposure Platform

The patterned light is converged to a focused image on a photoresist-coated substrate on the exposure platform. Typically, the light source is static – but the exposure platform has a motorized movement to enable the pattern to be replicated in one or multi-strips.

In recent innovations, DLP 'off' mirror light is also mined as a 'negative' image of the 'on' image pattern – and it is also processed via a complimentary optical system onto a complementary target substrate on a complimentary exposure platform (Patent No. US6238852B1/en, 2001).

If the 'on' image is processed via a positive (say) photoresist coating on the substrate on the original exposure platform, the 'Complimentary c-On' image is processed via negative photoresist coating on the substrate on the complimentary exposure platform. This effectively uses the otherwise lost 'off' beam dump and doubles the throughput of the Maskless Digital tool.

By implementing an optimized sub-pattern construction algorithm, the resulting pixel blending can further improve the edge smoothness of the litho pattern by an order of magnitude (Chen, 2017). Algorithms can also improve pattern stitching quality (Zhou, 2021).

IV. Future Directions and Conclusion

When it comes to photolithography, arguably the most important specification is the resolution of the system (measured as the critical dimension). A critical dimension of a lithographic system is the smallest distinct feature size that can be created in a definitive way in the patterning process. A smaller critical dimension is required for manufacturing smaller semiconductor nodes.

The achievable critical dimension is defined by the Rayleigh Criterion, which describes how the critical dimension is proportional to the exposure wavelength of light. Another characteristic of the critical dimension is that the larger the numerical aperture of the litho-optical system, the smaller the critical dimension. These relationships are captured in the following expression

$$C_D = k1 \cdot \lambda / NA$$

C_D - the critical dimension- is the resolution to which the smallest distinct feature size can be patterned using a light source of wavelength λ. NA -the numerical aperture – characterizes the optical system and is linked to the size of the lens system. In the above expression, k1 is a (process constant) coefficient. It is a function of the various factors related to the chip manufacturing process.

Historically, as semiconductor nodes have scaled down, photolithography has reduced the critical dimension by decreasing the wavelength of used light. However, as the industry stands today, further decreasing wavelength requires entirely new lithographic technologies like extreme ultraviolet (EUV).

While researchers and manufacturers have been hard at work to bring about shorter wavelengths, they've also investigated ways to reduce the k1 factor. To do this, one of the most powerful and important techniques has been computational lithography.

Computational lithography uses algorithmic models of the manufacturing process to compensate for manufacturing defects. Computational lithography enables optimization of the photomask by using an algorithm that deforms the image patterns (for example, at the corners of a rectangle block or a line) to compensate for physical and chemical effects/distortions that naturally occur in the conventional process. By doing this, computational lithography results in more accurate photolithography. In the context of Rayleigh's Criterion, this equates to lowering the k1 value and, hence increasing the critical dimension.

NVIDIA has recently announced cuLitho, which is a library of algorithms for computational lithography (NVIDIA, 2023). The library accelerates computational lithography by over 40 times. This innovation was enabled by NVIDIA (the AI GPU leader) in collaboration with industry leaders such as ASML (world's #1 lithography equipment company), TSMC (world's largest foundry), and Synopsys (a world-leading EDA developer).

The new library is an extension of NVIDIA's CUDA library optimized for the workloads associated with computational lithography. Consisting of tools and algorithms for GPU acceleration, cuLitho claims to speed up the manufacturing process for semiconductors by orders of magnitude over CPU-based methods. NVIDIA is claiming a 40x speed up of inverse lithography with cuLitho, resulting in 3x to 5x more masks being generated per day than possible with CPU systems.

Computational lithography uses two main technologies today: OPC (optical proximity correction) and ILT (inverse lithography technology). ILT is more advanced than OPC, but more computationally expensive. CuLitho should help enable more widespread use of ILT techniques, which allow more of the wafer area to be in focus, improving yield and reducing cost per chip.

Both OPC and ILT require data center levels of computing, either in a mask fabrication company or in the foundry. The implications of cuLitho are seemingly significant, resulting in semiconductor manufacturing that is faster, cheaper, and more accurate while aiming to keep Moore's law alive. So far, NVIDIA says that ASML, TSMC, and Synopsys have already adopted cuLitho, and they anticipate more major fabs will follow suit soon. Future

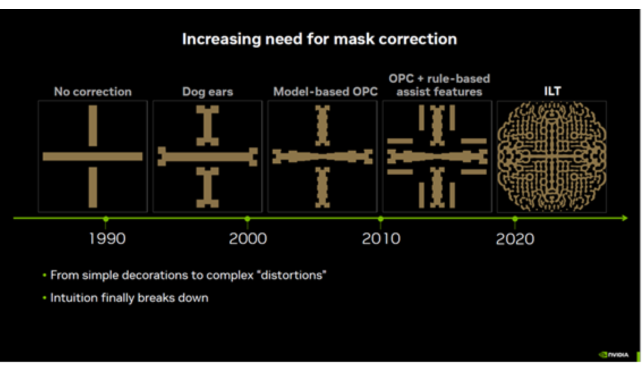

Figure 1: Use of algorithms for patterning corrections in Lithography, Source: NVIDA

directions on these technologies are captured in Table 2.

EUV lithography has been grabbing the limelight in patterning technologies as it delivers reduced geometries and captures the imagination of the press and techno-maniacs. However, this discussion of different patterning technologies brings out the complimentary positioning of other technologies for specific applications.

Maskless Digital Lithography is presented as a promising tool that compliments other techniques and can find application in MEMS and Advanced Semiconductor Packaging with less demanding geometries.

A combination of imaging algorithms and advancing lithography techniques are delivering the chip design as an image pattern on the wafer substrate. Converting that image pattern into physical architecture features (via semiconductor manufacturing processes) is what finally creates the semiconductor chips that shape our lives today.

V. Acknowledgments and Declaration of Interest

This paper is compiled as part of MTech Project work and focuses on a quick comparative on the patterning techniques in micro-electronics manufacturing processes. Maskless Digital Lithography is presented as a promising tool that compliments other techniques and can find application in MEMS and Advanced Semiconductor Packaging with less demanding geometries. While the scholar is supported by Applied Materials India Pvt Ltd (Indian subsidiary of Applied Materials, USA) under its continuous learning program, there is no involvement of Applied Materials in the project work or in the reports/ papers that result from it.

Table 2. Mask Based Lithography vs Maskless Pixel-blending Digital Lithography.

Types / Items	Mask-Based Lithography	Pixel-Blending Digital Lithography
Resolution	k_1 (λ / NA) Nikon: λ=365nm *i*-line, NA=0.11, 2.00μm pitch resolution → $k_1 = 0.60$ 1.50μm pitch resolution → $k_1 = 0.45$ 1.25μm pitch r → cannot resolve Marginal diffraction orders – when $k_1 \leq 0.60$ OPC required to improve corner printing Poor sidewall tapers	k_0 (Projected Imaging Pixel Pitch) No OPC needed for better corner printing Digitally tunable sidewall tapers
DOF	$\pm k_2$ (λ / NA^2)	$\pm k_2$ (λ / NA^2)
Future Directions	EUV systems (shorter wavelengths) and specialized optics control NA to deliver lower resolutions; OPC improvements refine the structure definition; There is also focus on process constant innovations to improve resolution	Focus on improved resolution via next generation DLP (expected to improve from 2000nm resolution to 500nm resolution); innovation in optics and integration algorithms to improve the resolution

λ : wavelength of light beam in the litho system; NA is Numerical Aperture of the Optical system used in the litho process; k are process constants; DOF = Depth of Field

Source: Adapted using data from Nikon Lithography tool database

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