https://doi.org/10.58864/mrijet.2023.10.2.4

A Comparative Analysis of VS-CNTFET and CMOS Based Inverter Circuit

Shashank Gaur
Research Associate, Department of Electrical & Electronics Engineering, SET,
Manav Rachna International Institute of Research and Studies,
Faridabad, Haryana, India
Email:shashank.gaur87@gmail.com

Dr. Umesh Dutta
Associate Professor, Department of Electronics and Communication Engineering, SET,
Manav Rachna International Institute of Research and Studies, Faridabad,
Haryana, India
Email: umeshdutta.set@mriu.edu.in

Abstract: *This abstract delves into the comparative exploration between Carbon Nanotube Field Effect Transistors (CNTFETs) and traditional CMOS (Complementary Metal-Oxide-Semiconductor) transistors, with a specific emphasis on digital inverter circuits. Utilizing carbon nanotubes derived from the graphene allotrope, CNTFETs are introduced as a technological advancement, providing advantages such as reduced size and lower power consumption. The investigation centres on the evaluation of the Stanford model, particularly focusing on the Virtual Source Carbon Nanotube Field Effect Transistor. This specific model showcases superior performance, compact dimensions, and decreased power requirements when contrasted with silicon-based MOSFETs. The analytical process involves subjecting virtual source CNTFET inverter circuits and MOSFET-based circuits to testing via the Symica software tool, encompassing the examination of transient response, voltage transfer characteristics, and steady-state power consumption. The outcomes underscore the potential of CNTFETs as promising alternatives in the progression of digital design, offering heightened efficiency and diminished power consumption.*

Keywords: *CMOS, CNT, CNTFET, VS-CNTFET, VS-CNTFET Inverter*

I. INTRODUCTION

Carbon Nanotube Field-Effect Transistors (CNTFETs) represents a paradigm shift from traditional MOSFETs due to their utilization of one-dimensional cylindrical semiconducting carbon nanotubes as conduits for current flow, replacing N or P channels found in conventional transistors. Their unique structure enriches them with superior electron transport capabilities, facilitated by high carrier mobility and ballistic transport characteristics within narrow nano-scale channels. This microscopic scale grants CNTFETs enhanced gate control, minimizing Short Channel Effects (SCEs) and ensuring ultra-fast switching rates, reduced power consumption, and improved device performance [1].

CNTFETs offer distinct advantages over shrinking silicon MOSFETs, which suffer from increased power consumption and various short-channel effects [2], leading to mobility degradation and low driving current. CNTFETs excel in scalability [3], harnessing the atomically thin nature of carbon nanotubes and enabling the synthesis of nanometre-sized diameters ideal for advanced nanoelectronics applications. Their miniature dimensions promise the development of denser, more compact integrated circuits [4] capable of handling vast amounts of data in cutting-edge computing systems.

Nevertheless, challenges arise in accurately capturing dimensional effects, series resistance, and tunneling leakage current in compact models, impacting device performance and measurement variations. Achieving constant input parameters remains crucial to mitigate these issues and enable scaling-free device design, allowing for a comprehensive study of measurement variations and scaling effects [5].

Within the realm of the Virtual Source CNTFET semi-empirical model, understanding the determinants of current magnitude is essential. Fig. 1

 © 2023 MRIJET, MRIIRS

illustrates the thermionic flux of electrons over the barrier, where lateral electric field considerations, charge density, and velocity collectively determine drain current per unit width. The gradual channel effect plays a significant role, specifically applied at the Virtual Source (VS) [6].

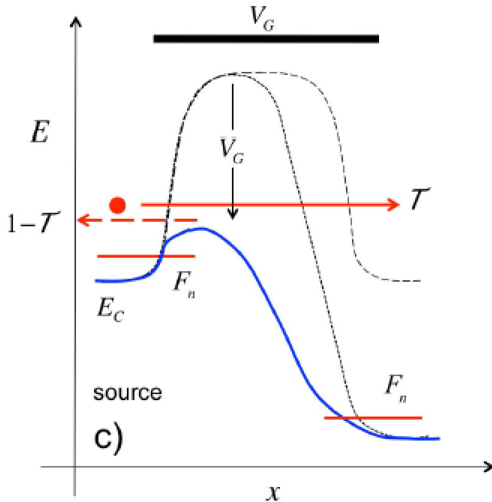


Figure 1: VS-CNTFET showing conduction band edge versus position for a large gate and drain bias

Transitioning to CNTFET Inverters (as depicted in Fig. 2), these devices leverage gate voltage manipulation to toggle between states, utilizing P-CNTFET and N-CNTFET configurations to regulate output values based on binary inputs [7]. This inverter circuit, akin to CMOS but with superior performance and lower power consumption, operates seamlessly with binary logic, providing high noise immunity and delivering ideal output values corresponding to input voltages ranges.

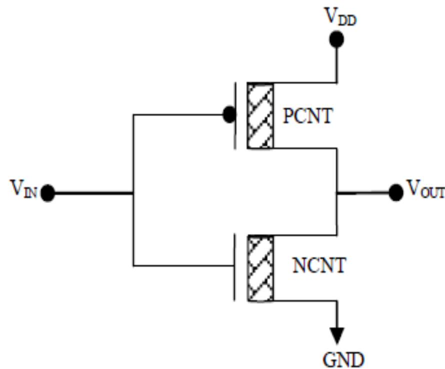


Figure 2: CNTFET Inverter

CNTFET-based inverters showcase a captivating potential within the realm of digital electronics, upholding remarkable noise margins while adeptly converting input voltages into precise binary digits. This pioneering technology stands as a profound leap forward in the landscape marking of digital design, commencing a noteworthy advancement in its domain.

II. RELATED WORK

We have looked at lots of papers before diving into our research. These papers covered different ideas and ways of studying things. Our goal is adding something new based on what we have learned from these papers and fill in any missing pieces.

Radamson H H et al. [8] demonstrated the continued functionality of a traditional MOSFET up to 100 nm. As channel lengths decrease in accordance with scaling trends, a number of undesirable side effects emerge. The electrical performance of the device and the impacts of short channels should be decreased as a result of the scaling of microelectronic technologies. Djeffal et al. [9] released a study on gate-all-around-junction-less MOSFETs (GAAJ). A lot of doping occurs in the source and drain extensions of this arrangement as opposed to the channels. The drain current is enhanced by including the strongly doped extensions. The current through the GAAJ MOSFET with extensions is much higher than that via the standard GAAJ. The ion current magnitude has risen by 70% in the heavily doped areas. Ouruji et al. [10] put forth a DSBO SOI MOSFET, which stands for double-step buried oxide. The best features of bulk MOSFETs and SOI structures are combined in this design. The goal of this design is to decrease self-heating by lowering the thickness of silicon dioxide and altering the form of the buried oxide into a double-step pattern. Regardless of the self-heating effects, the drain current increases in this configuration. Kwon et al. [11] offered a study on silicon-based MOSFETs to enhance performance in hot conditions. Applications in extreme environments are ideal for the MOSFET. Inserting wide band gap material locally between the source and channel areas allows for high-temperature functioning. To stop current from leaking out of the substrate, the suggested SOI MOSFET design uses buried oxide (BOX).

Kumar et al. [12] suggested a recessed channel MOSFET without a black phosphorus junction. Incorporated inside the junction-less recessed

MOSFET is black phosphorus. A drain current of up to 0.3 mA may be seen in this configuration. The sub-threshold slope improves, and the OFF current decreases. The ON current is strong, and the OFF current is low in the black phosphorus material. Djeffal et al. [13] suggested a 10 nm gate MOSFET with two materials around it for use in digital applications. This optimization method combines the best features of multi-objective genetic
MOSFETs. The electrical behaviour of 10 nm DMSG MOSFET is optimised and improved using the MOGAs method. This enables digital applications with nanoscale speed and minimal power consumption. Pang et al. [14] suggested a low voltage application arrangement for 0.1 µm n-MOSFET pockets. Within this structure, a substantially doped pocket area is built around the drain and a source region, while a mildly doped center region is produced in the middle. This layout not only satisfies the requirements for both the ON and OFF currents, but it also offers excellent protection from short-channel effects. Saramekala et al. [15] suggested a metal-gate, one-channel MOSFET with recessed sources and drains made of silicon on insulator. This gadget has a low DIBL value and a high ON current. While the drain and source regions are strongly doped, the channel area is moderately doped. Direct metal contact at the source and drain sides characterizes the Schottky barrier-CNTFET channel, which contains intrinsic carbon nanotubes. Due to the channel's inherent nature, ambipolar features are noted. Several methods are used to resist ambipolar effects [16]. The most significant issue with SB-CNTFET is that the magnitude of the inverse sub-threshold slope is often greater than the theoretical threshold, which is 60 mV/dec [17].

Partially gated CNTFET is the second type, where the channel is uniformly doped or intrinsic (p or n). As uniform doping exists throughout the channel, the device works in depletion mode. They display n-type or p-type behavior depending on the doping type. There is an improvement in the device characteristics with ohmic contacts. In such devices, the ION is limited by a source exhaustion phenomenon [18]. Schottky barriers are created at the source and drain region when the channel is intrinsic throughout, though the effects of the Schottky barriers are not significant due to the partial gate. It also operates in enhancement mode.
Second, there is the partially gated CNTFET, which uses an intrinsic or uniformly doped channel (p or n). The gadget operates in depletion mode because the doping is homogeneous across the channel. Depending on the kind of doping, they exhibit either n-type or p-type behaviour. The device's properties are enhanced when ohmic contacts are used. The ION in these devices is limited by a process known as source exhaustion. When the channel is intrinsic all the way through, Schottky barriers are formed at the source and drain regions; however, the partial gate makes their effects insignificant. It can also function in an enhanced mode.

The third type is C-CNTFET. The structure is similar to conventional MOSFET, so it is called conventional CNTFET. The ungated channel comprises intrinsic CNTFET, while the source and the drain are doped heavily. There is an improvement in the device characteristics as a result of doping, with unipolar properties being observed at low OFF current (IOFF). The ION is also limited by the quantity of charge that may be induced by the gate in the channel and not by the source doping [19]. Due to the deficiency of the Schottky barrier, the OFF current is limited by thermal emission rather than direct tunneling, which gives appreciable inverse sub-threshold slope values (60 Mv/dec).

Type four is T-CNTFET. Using the CNT channel to introduce a p-i-n or n-i-p doping profile results in a T- CNTFET structure. The T-CNTFET moniker comes from the fact that the device operates using the tunnelling principle. Tunneling behavior, although harmful in CNTFETs, may be useful in T-CNTFETs when controlled by the gate voltage [20]. According to [21], the gate voltage controls the band-to-band tunneling current. At normal temperatures, T-CNTFETs achieve an inverted sub-threshold slope of less than 60 mV/dec, which is their main advantage. But getting tunnel devices made is not without its share of obstacles [22].

III. PROPOSED APPROACH

The utilization of the Symica software tool has enabled an intricate exploration of simulations within the 32-nanometer parameter transistor model technology node. Focusing on the fundamental inverter circuit, which serves as the cornerstone of single-bit binary-based digital design, comprehensive investigations were conducted for both CMOS and VS-CNTFET configurations.

In Case 1, the transient response of the CMOS was meticulously examined. Employing a 32-nanometer length and 1-micrometer width for both the PMOS and NMOS transistors, a vivid analysis was conducted with a voltage application of 500mV to the PMOS source while the NMOS source was connected to the ground. Through interconnected gate operations and the application of a square wave with distinct high and low voltages of 500mV and 0V, respectively, the rise and fall times of 1 nanosecond were observed, coupled with a pulse width of 9 nanoseconds and zero pulse delay.

The resultant output generated an inverted square wave.

Similarly, for the VS-CNTFET configuration, utilizing identical dimensions but with a cylindrical tube of 1.2-
nanometer diameter, successful simulations were executed using Stanford-written HSPICE code, although with minor ripples that were mitigated through the incorporation of parasitic capacitance within the interconnects.

Moving to Case 2, the focus shifted to the Voltage Transfer Characteristics (VTC) curve for both CMOS and VS-CNTFET configurations. In the CMOS setup, the VTC curve was obtained by connecting the PMOS source to a positive 500mV source, while the NMOS source was linked to ground. The interconnected gate of both transistors received a positive 500mV voltage source, yielding a steady-state DC response and the subsequent calculation of noise margins—262.83mV for the High state and 191.03mV for the Low state. The VS-CNTFET VTC curve was simulated using Stanford HSPICE, leading to a High state Noise Margin of 220.58mV and a Low state Noise Margin of 196.58mV.

Lastly, in Case 3, the steady-state leakage current for both CMOS and VS-CNTFET setups was meticulously evaluated. In the CMOS scenario, a square wave input with specific high and low parameters was applied, resulting in a calculated leakage current of 1.0701-nanoampere. Conversely, leveraging Stanford HSPICE code, the VS-CNTFET leakage current was simulated, yielding a leakage current of .2957-nanoampere.

These comprehensive analyses and simulations using Symica software for CMOS and Stanford HSPICE for VS-CNTFET configurations have provided detailed insights into transient responses, VTC curves, noise margins, and steady-state leakage currents, highlighting the performance and characteristics of these crucial digital design components at the cutting edge of technology nodes.

IV. EXPERIMENTAL EVALUATION

The mastery of Symica software truly comes alive in its application for simulations. Every simulation performance was carefully organized using the 32-nanometer parameter transistor model technology, serving as a complex canvas upon which the symphony of the inverter circuit unfolded. This circuit, the fundamental cornerstone of single-bit binary-based digital designs, represents the essence of technological innovation, seamlessly weaving together elegance and precision.

1. **Transient response for CMOS**

The Figure 3 is designed to study the transient response of CMOS based inverter model. For the analysis of transient response, we have applied square wave clock to the gate of the CMOS Inverter representing the High 1 and Low 0. High is 500mV and Low is 0-V. High & Low pulse width is 9-nSec and complete width cycle is 20-nSec.

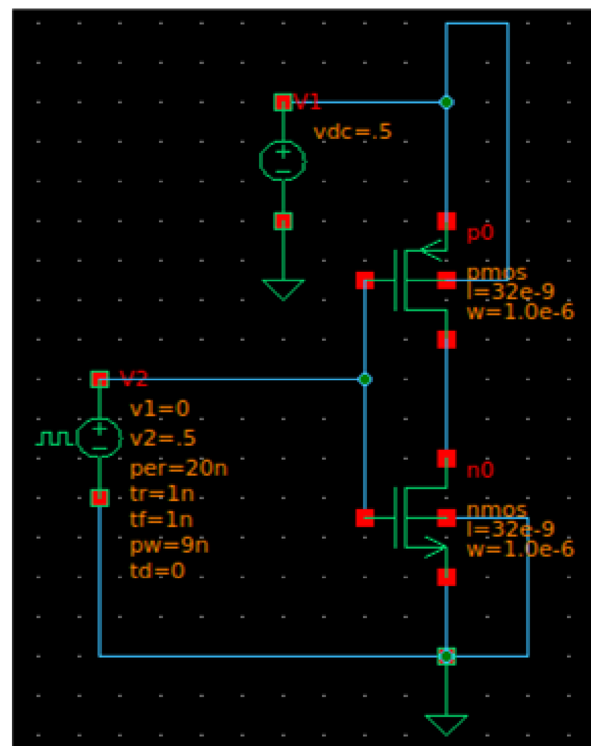


Figure 3: CMOS Transient Response Circuit

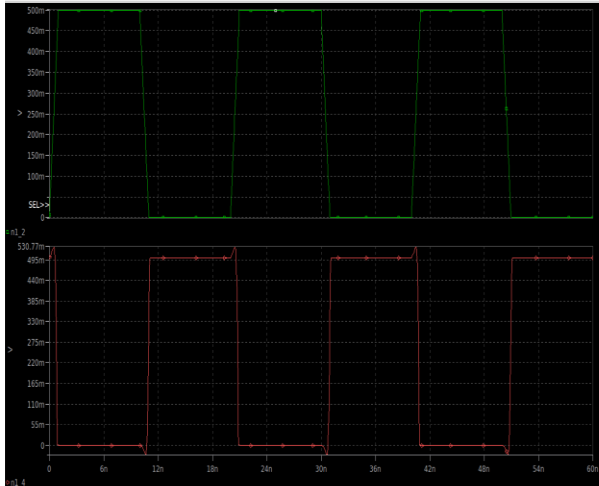


Figure 4: CMOS Transient Response Output

Figure 4 shows the graph of the Input and output transient square waveforms in which the Green one represents the Input square wave and the Red one represents the output square wave. The output shows an inverse relationship with the input, where high input results in low output, and conversely, low input yields high output. Hence complementary binary bits 1 and 0 are being generated, which solves our purpose of the basic building block of our bit-based digital design.

For VS-CNTFET: The provided Stanford SPICE code has undergone simulation.

```
1   * VSCNFET : fan-out inverter  transient simulation
2
3   .options apb
4
5   .param   Temperature=298.15k
6   .hdl 'vscnfet_1_0_1.va'
7
8   .param supply=.5
9   .param fo=4
10  .param tcyc=300p
11  .param trf=1p
12  .param Lg=32e-9
13  .param Lc=12.9e-9
14  .param Lext=3.2e-9
15  .param s=10e-9
16  .param Hg=20e-9
17  .param W=1e-6
18  .param Geomod=1
19  .param SDTmod=1
20  .param BTBTmod=1
21  .param Rcmod=1
22  .param Rs0=0
23  .param Vfbn=0.09
24  .param Vfbp=-0.09
25  .param D=1.2e-9
26
27  .subckt inv vdd in out
28  xn out in gnd vscnfet_1_0_1 FETtype=1
29  +Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbn D=D
30  +SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
31  xp out in vdd vscnfet_1_0_1 FETtype=-1
32  +Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbp D=D
33  +SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
34  .ends inv
35  x1 vdd ck in inv m=1
36  x2 vdd in out inv m='fo'
37  x3 vdd out n1 inv m='fo*fo'
38  x4 vdd n1 n2 inv m='fo*fo*fo'
39  //cic out gnd 'cic*fo*fo'
40  vdd vdd gnd 'supply'
41  vck ck gnd pulse 0 'supply' 'tcyc/2' trf trf 'tcyc/2-trf' tcyc
42  .tran 0.1p 'tcyc*3'
43  .end
```

Output for VS-CNTFET

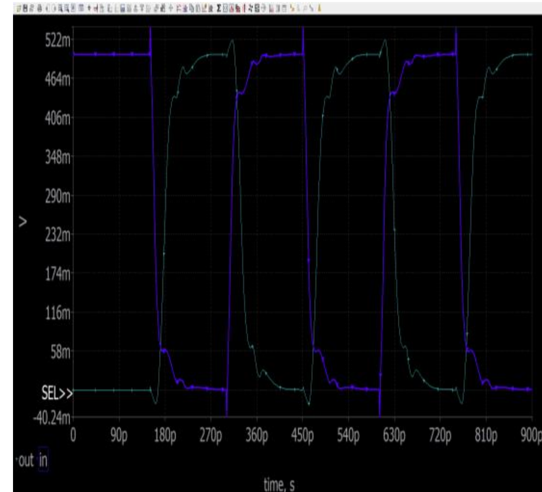


Figure 5: VS-CNTFET Transient Response Output

In the Figure 5, where blue lines are representing input pulse and green one is representing output pulse. They are behaving as a square wave of an inverter circuit with the output pulse as a complementary of input pulse. Hence our purpose of generating binary bits is completed.

2. Voltage Transfer Characteristics Curve (VTC) for CMOS

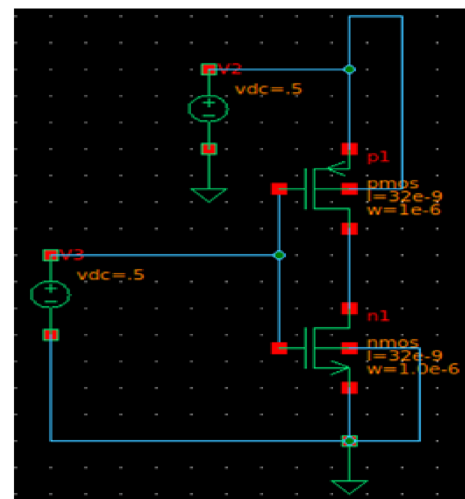


Figure 6: VTC Circuit Design

The Figure 6, circuit has been made to study the voltage transfer characteristics of the CMOS based inverter circuit. In the above circuit one DC voltage source of 500mV connected to the input of both the Gate of the inverter circuit and the source side of the pullup PMOS is connected with the positive side of

500mV DC supply and the source of NMOS is connected to the ground.

Output for CMOS

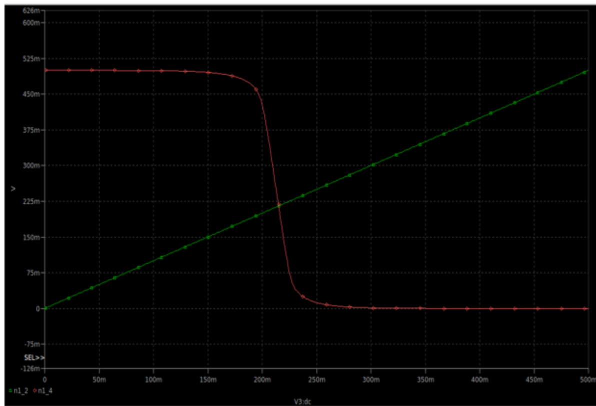


Figure 7: VTC Output Response

The above shown Figure 7, shows graph which is the VTC curve of a CMOS inverter, it is a graphical representation of its input-output relationship. It depicts the behaviour of a standard CMOS inverter, where the output voltage (V_{out}) undergoes a transformation based on fluctuations in the input voltage (V_{in}). In this configuration, a low input voltage (0) results in a high output (1), while a high input voltage (1) corresponds to a low output (0).

For VS-CNTFET

Given below the Stanford HSPICE code has been used to draw VTC curve

```
* VSCNFET : inverter transfer curve

.options POST

.param   TEMP=25
.hdl 'vscnfet_1_0_1.va'

.param supply=.5
.param Lg=32e-9
.param Lc=12.9e-9
.param Lext=3.2e-9
.param s=10e-9
.param Hg=20e-9
.param W=1e-6
.param Geomod=1
.param SDTmod=1
.param BTBTmod=1
.param Rcmod=1
.param Rs0=0
.param Vfbn=0.09
.param Vfbp=-0.09
.param Dia=1.2e-9

xn out in gnd vscnfet_1_0_1 FETtype=1
+Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbn dcnt=Dia
+SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
xp out in vdd vscnfet_1_0_1 FETtype=-1
+Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbp dcnt=Dia
+SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
vdd vdd gnd 'supply'

vin in gnd 0

**********************************************************************
* Measurements
**********************************************************************
.DC      vin   START='0'     STOP='supply'   STEP='0.01'

.end
```

Output for VS-CNTFET

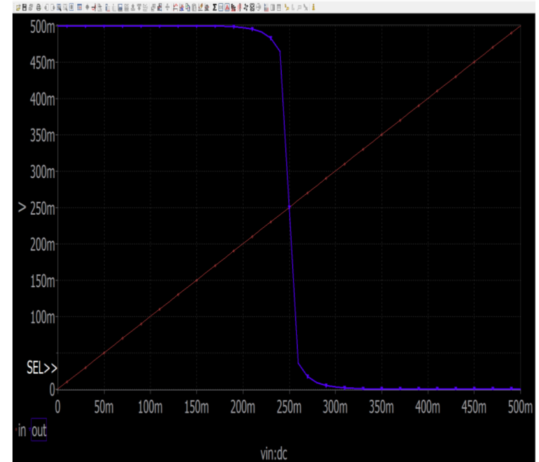


Figure 8: VS-CNTFET VTC Response

The above shown Figure 8, is the VTC curve of a CNTFET inverter, it is a graphical representation of its input-output relationship. It illustrates how the output voltage (Vout) changes in response to variations in the input voltage (Vin). In a typical CNTFET inverter, when the input voltage is low (0), the output is high (1), and when the input is high (1), the output is low (0). The VTC curve is divided into two regions: the saturation region and the cut-off region. In the saturation region, the transistor that is ON operates in its saturation mode, providing a low-resistance path between V_{DD} and the output. In the cut-off region, the transistor that is OFF has a high resistance, effectively disconnecting the output from V_{DD}.

3. Steady State Leakage Current for CMOS

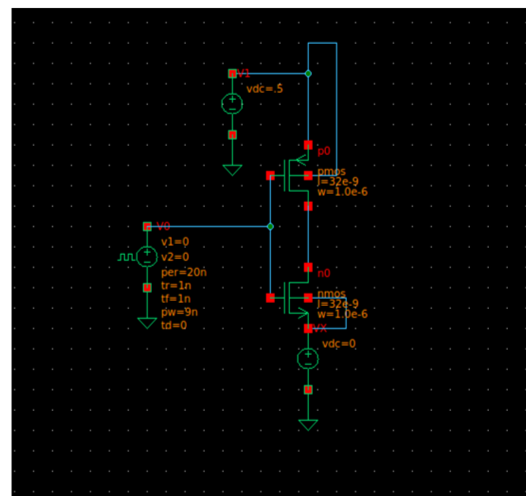


Figure 9: Circuit for Steady State Leakage Current

In Figure 9, circuit is made to find out steady state

leakage current for CMOS based inverter circuit. At the Gate input side of the circuit we have applied 0 Volt pulsating clock. At the source end of the pull up PMOS transistor we have applied 500mV positive DC supply. At the source end of the pull-down NMOS transistor, we have applied a virtual voltage DC supply of value 0 Volts. Now the circuit transient response is simulated and its netlist is exported as can be seen below.

```
// Title: "/home/tcadlab/Desktop/ece/sh7"
// Generated by   : Symica
// (c) 2009-2020 Symica. All rights reserved. (www.symica.com)
// Generated on   : Sat Aug 19 15:38:58 2023

simulator lang=local


global 0

include "/home/tcadlab/Downloads/model files ptm/32 nm cmos.txt"

V1_0 n1_3 0 vsource type=dc dc=.5
n0_1 n1_4 n1_2 n2_3 n2_3 nmos w=1e-06 l=3.2e-08
VX_2 n2_3 0 vsource type=dc dc=0
p0_3 n1_4 n1_2 n1_3 n1_3 pmos l=3.2e-08 w=1e-06
V0_4 n1_2 0 vsource type=pulse delay=0 val0=0 val1=0 period=2e-08 rise=1e-09 fall=1e-09 width=9e-09
TimeSweep tran start=0 stop=4e-08 lteratio=3.5
save n1_4 Vx_2:currents

saveOptions options save=all currents=selected

DEFAULT_OPTIONS options tnom=25 temp=25  fast_spice=0 reltol=1.000000e-03
```

The above exported file is simulated using the code "symspice -i title of the file"

Given below the following value of steady state leakage current has been obtained

```
#nodeset
n1_3     5.000000e-01
n2_3     0.000000e+00
n1_2     0.000000e+00
n1_4     4.999840e-01
n0_1:5   1.935334e-09
n0_1:6   9.563771e-13
n0_1:7   4.303069e-12
n0_1:8   4.787817e-13
p0_3:5   7.256952e-11
p0_3:6   5.000000e-01
p0_3:7   5.000000e-01
p0_3:8   5.000000e-01
V0_4:3   2.710670e-10
V1_0:3   -1.341235e-09
VX_2:3   1.070168e-09
```

For VS-CNTFET

Given below the Stanford HSPICE code for simulation to find out the steady state leakage current.

```
1  * VSCNFET : fan-out inverter Leakage Power transient simulation
2
3  .options apb
4
5  .param   Temperature=298.15k
6  .hdl 'vscnfet_1_0_1.va'
7
8  .param supply=.5
9  .param supply1=0
10 .param fo=4
11 .param tcyc=300p
12 .param trf=1p
13
14 .param Lg=32e-9
15 .param Lc=12.9e-9
16 .param Lext=3.2e-9
17 .param s=10e-9
18 .param Hg=20e-9
19 .param W=1e-6
20 .param Geomod=1
21 .param SDTmod=1
22 .param BTBTmod=1
23 .param Rcmod=1
24 .param Rs0=0
25 .param Vfbn=0.09
26 .param Vfbp=-0.09
27 .param D=1.2e-9
28
29 xn out in 2 vscnfet_1_0_1 FETtype=1
30 +Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbn D=D
31 +SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
32 xp out in vdd vscnfet_1_0_1 FETtype=-1
33 +Lg=Lg Lc=Lc Lext=Lext s=s Hg=Hg W=W Geomod=Geomod Vfb=Vfbp D=D
34 +SDTmod=SDTmod BTBTmod=BTBTmod Rcmod=Rcmod Rs0=Rs0
35
36 vx 2 gnd 0
37 vck in gnd pulse 0 0 'tcyc/2' trf trf 'tcyc/2-trf' tcyc
38 *vck in gnd dc .5
39 vdd vdd gnd 'supply'
40 .tran 0n 40n
41 .print I(vx)
42
43 .end
```

Output for VS-CNTFET

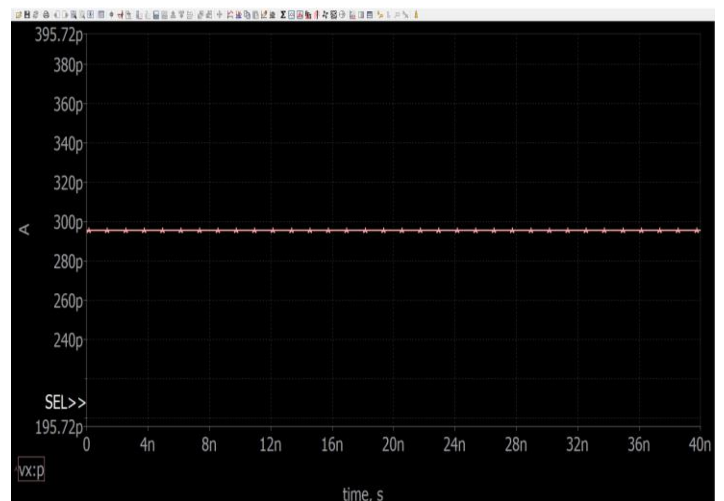


Figure 10: VS-CNTFET Steady State Leakage Current

V. RESULTS

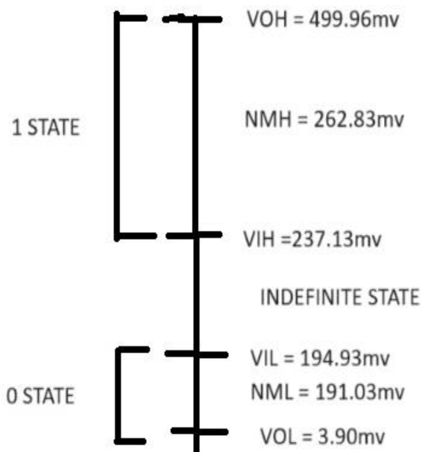
Steady State Power consumed for CMOS

Steady State Leakage Current = 1.0701nA
V = 500mV
I = 1.0701nA
Power = V.I
Leakage Power = 0.53505nW

Steady State Power consumed for VS-CNTFET

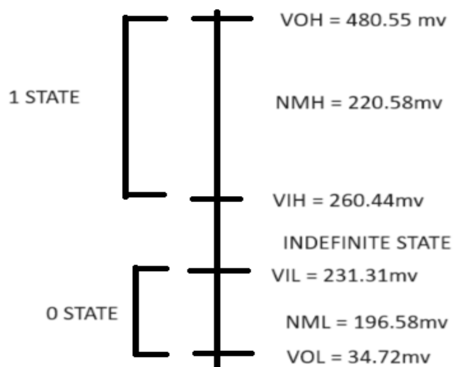
Steady State leakage Current = .2957nA
Leakage Power = V.I
V = 500mV
I = .2957nA
Leakage Power = 0.14785 nW

Reduction in Leakage Power as compared to CMOS = 27%



Noise Margin for CMOS

Noise Margin for VS-CNTFET



VI. CONCLUSION

The main focus of the International Technology Roadmap for Semiconductor (ITRS) is continuous progress in the field of the electronics, with an aim of new small scale device design that consumes less power, robust in nature and that can be easily implemented in the modern state of the art electronics designs. With evidently use of MOSFET based devices to reduce power consumption by scaling them downwardly faces many short channel effects that affect its performance. This gave rise to the modern era of nanoelectronics. In which case a new emerging device named as Carbon Nanotube Field Effect Transistor (CNTFET) is a promising device on which various research are going on.

We have simulated the 32-nm technology node based two electronic devices, conventionally used CMOS and Carbon Nanotube Field Effect transistors (CNTFET). The 32-nm technology node based CNTFET is considered based on its use in space application, where radiations and various frequency based noise is present.

We have successfully caried out the simulation on both the devices and founded that CNTFET is consuming 27% less power as compared to its CMOS counterpart which is very beneficially of its use in space applications.

VII. LIMITATIONS AND FUTURE WORK

A. Limitations

1. Fabrication Challenges: When it comes to large-scale integration, CNTFET manufacture is still a difficult and expensive procedure. At wafer size, it is still difficult to produce high-quality, aligned CNTs.

2. Chirality Dependence: Because of their chirality dependence, CNTs' electrical characteristics can vary greatly throughout varieties in terms of conductance and electronic characteristics. This may make device consistency and performance more difficult.

3. Contact Resistance: CNTFET performance may be limited by high contact resistance between the metal electrodes and CNT. It is essential to develop contact technology that is scalable, repeatable, and low resistance.

4. Defects and Impurities: The electrical

characteristics of CNTs may be impacted by flaws and contaminants. To achieve high-performance CNTFETs, these flaws must be
reduced and controlled.
5. Integration with Existing Technology: One major problem is integrating CNTFETs with current silicon-based technologies. Practical applications require mixed-technology systems to be reliable and compatible.

B. Future Work

1. Improved Fabrication Techniques: The main goal will be to create more dependable, scalable, and affordable processes for the synthesis of CNTs and the manufacture of devices. Additional refining is required for techniques like
chemical vapour deposition (CVD) and sorting procedures.
2. Chirality Control: Enhancing techniques to choose and regulate the chirality of carbon nanotubes (CNTs) in transistors will contribute to increased device performance and consistency.
3. Contact Engineering: CNTFET performance may be enhanced overall and contact resistance can be decreased by investigating novel contact materials and methods.
4. Defect Mitigation: Enhancing the quality and dependability of CNTFETs will require locating and reducing flaws and contaminants in CNTs.

VIII. REFERENCES

[1] Lee CS, Pop E, Franklin AD, Haensch W, Wong HS. A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime—Part I: Intrinsic elements. IEEE transactions on electron devices. 2015 Aug 3; 62(9):3061-9.

[2] Khakifirooz A, Nayfeh OM, Antoniadis D. A simple semi empirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters. IEEE Transactions on Electron Devices. 2009 Jul 10; 56(8):1674-80.

[3] Lee CS, Pop E, Franklin AD, Haensch W, Wong HS. A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime—Part II: Extrinsic elements, performance assessment, and design optimization. IEEE Transactions on Electron Devices. 2015 Aug 14; 62(9):3070-8.

[4] Najari M, Frégonèse S, Maneux C, Mnif H, Masmoudi N, Zimmer T. Schottky barrier carbon nanotube transistor: Compact modeling, scaling study, and circuit design applications. IEEE transactions on electron devices. 2010 Oct 28; 58(1):195-205.

[5] Zhang J, Lin A, Patil N, Wei H, Wei L, Wong HS, Mitra S. Carbon nanotube robust digital VLSI.IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2012 Mar 19; 31(4):453-71.

[6] Lee CS, Wong HS. Virtual-source carbon nanotube field-effect transistors model. Version.2015; 1(0):1.

[7] Farhana S, Alam AZ, Khan S. CNTFET inverter: A high voltage gain logic gate. In2014 IEEE International Conference on Smart Instrumentation, Measurement and Applications (ICSIMA 2014 Nov 25 (pp. 1-4). IEEE.

[8] Radamson, Henry, et al. CMOS past, present and future. Woodhead Publishing, 2018.

[9] Djeffal F, Ferhati H, Bentrcia T. Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions. Superlattices and Microstructures. 2016 Feb 1; 90:132-40.

[10] Orouji AA, Heydari S, Fathipour M. Double step buried oxide (DSBO) SOI-MOSFET: A proposed structure for improving self-heating effects. Physica E: Low-dimensional Systems and Nanostructures. 2009 Sep 1; 41(9):1665-8.

[11] Kwon I, Kwon HI, Cho IH. Development of high temperature operation silicon based MOSFET for harsh environment application. Results in Physics. 2018 Dec 1; 11:475-81.

[12] Kumar A, Tripathi MM, Chaujar R. Comprehensive analysis of sub-20 nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications. Superlattices and Microstructures. 2018 Apr 1; 116:171-80.

[13] Djeffal F, Lakhdar N, Yousfi A. An optimized design of 10-nm-scale dual-material surrounded gate MOSFETs for digital circuit applications. Physica E: Low-dimensional Systems and Nanostructures. 2011

Oct 1; 44(1):339-44.

[14] Pang YS, Brews JR. Design of 0.1-μm pocket n-MOSFETs for low-voltage applications.Solid-State Electronics. 2002 Dec 1;46(12):2315-22.

[15] Pal A, Sarkar A. Analytical study of dual material surrounding gate MOSFET to suppress short- channel effects (SCEs). Engineering Science and Technology, an International Journal. 2014 Dec 1; 17(4):205-12.

[16] Ossaimee M, Gamal S, Shaker A. Gate dielectric constant engineering for suppression of ambipolar conduction in CNTFETs. Electronics Letters. 2015 Mar; 51(6):503-4.

[17] Appenzeller J, Knoch J, Derycke V, Martel R, Wind S, Avouris P. Field-modulated carrier transport in carbon nanotube transistors. Physical review letters. 2002 Aug 29; 89(12):126801

[18] Guo J, Datta S, Lundstrom M, Brink M, McEuen P, Javey A, Dai H, Kim H, McIntyre P. Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors. InDigest. International Electron Devices Meeting, 2002 Dec 8 (pp. 711-714). IEEE.

[19] Chau R, Doyle B, Doczy M, Datta S, Hareland S, Jin B, Kavalieros J, Metz M. Silicon nano-transistors and breaking the 10 nm physical gate length barrier. In61st Device Research Conference. Conference Digest (Cat. No. 03TH8663) 2003 Jun 23 (pp. 123-126). IEEE.

[20] Appenzeller J, Lin YM, Knoch J, Chen Z, Avouris P. Comparing carbon nanotube transistors-the ideal choice: a novel tunneling device design. IEEE Transactions on Electron Devices. 2005 Dec 5; 52(12):2568-76
.
[21] Appenzeller J, Lin YM, Knoch J, Avouris P. Band-to-band tunneling in carbon nanotube field-effect transistors. Physical review letters. 2004 Nov 4; 93(19):196805.

[22] Avci UE, Morris DH, Young IA. Tunnel field-effect transistors: Prospects and challenges. IEEE Journal of the Electron Devices Society. 2015 Jan 12; 3(3):88-95.