

Swati Sharma
swati.sharma41@yahoo.com

Ashok Mittal
(Senior Member IEEE)
Principal, Ambedkar Institute of
Advanced Communication
Technologies and Research
Geeta Colony, India
ashok.mittal@yahoo.com

Mrs. Meena Mishra
(Scientist F)
Solid State Physical Laboratory
(DRDO)
meenamishra@hotmail.com

S.K. Tomar
(Scientist E)
Solid State Physical Laboratory
(DRDO)
sktomar123@gmail.com

Design and Analysis of Three Stages pHEMT - LNA at K-Band

Abstract: This paper represents the design of three stage LNA using EC2612 pHEMT technology. pHEMT technology gives high transconductance and shows better reliability. This three stage amplifier has been designed for K-band applications. The GaAlAs LNA is suitable for trans-receiver front end due to the low input output VSWR, high stability and redundancy. The LNA is designed at 21GHz using distributed parameters and over RT duroid ($\epsilon_r = 2.2$). This structure is simulated and fabricated using ADS software. The simulated result shows the minimum noise figure of 1.09dB and a maximum gain of 25dB. Here tuning is done for gain flatness and ± 0.5 dB gain flatness is achieved for the range of 20-22GHz. Hence, the simulated and fabricated results are in good agreement.

Index Terms— LNA, pHEMT technology.

I. Introduction

Nowadays, LNA is the key component in any front end receiver system. As the progress of front end receiver, the data rate has been speed up in several high frequency applications such as wireless communication, satellite communication, radar systems and smart antennas. These systems require low noise performance to deliver high speed data. At high frequency the circuit deviates from their actual behavior and are difficult to implement. Many researchers presented several LNA systems with operating frequency at S to X band [1,2,3] with wide band frequency characteristics.

In recent years, several LNA designs have been reported using pHEMT, MESFET and HBT technology using package type transistors. pHEMT technology is preferred in LNA front end receivers due to low noise, high gain, high transconductance and high reliability. This paper demonstrated LNA system using chip type transistors. The 3 stage LNA is designed using pHEMT technology which has 25dB of gain and 1.09dB of noise figure. Here source series inductor is used for better stability and tuning is done to improve gain flatness. The objective of this design is to obtain the low noise, high gain, good input/ output return loss, high reliability and miniaturization of the circuit. This design has several applications in commercial and defense systems.

II. Circuit Design

LNA is one of the most important building block of communication receiver system. The most important design considerations are stability and noise. So, here main function is to provide enough gain to overcome the noise of subsequent stages while adding as little noise as possible. Fig. 1 depicts the general block diagram of three stage LNA. The figure shows the RF source and RF output along with the matching circuit. Here, interstate matching used to connect the cascading of two or more transistor.

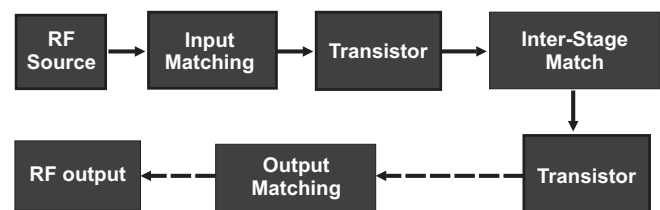


Fig.1. General block diagram of three stage LNA.

The 3 stage cascaded LNA operating with 2V power supply and drain current of 14mA was designed using EC2612 transistor. Fig 2 shows the schematic diagram of the amplifier circuit consisting of distributed parameters.

One of the important characteristics of an amplifier design is unconditional stability. Whereas Series

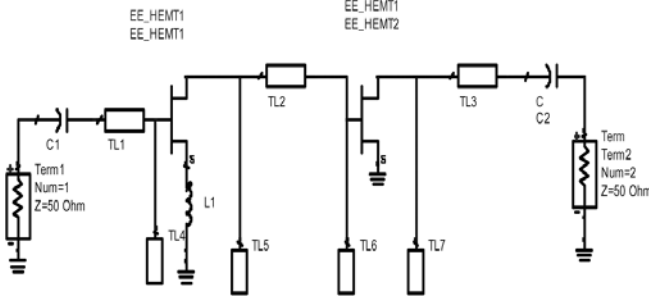


Fig. 2: Schematic diagram of LNA.

feedback inductor at source is placed to improve the amplifier stability. Inductive reactance should be as small as possible so that gain would be maximum. Source degeneration provides negative feedback so it reduces the effect of non linearity. Blocking capacitor was used at the input & output of every stage to resist the dc power entering into the transistor. In this design, pHEMT transistor of width $0.15\mu\text{m}$ is introduced at every stage and Microstrip lines are used for matching .Here the gain flatness was achieved by tuning of output matching circuit.

The characterization of transistors has been done using S-parameters. The device parameters at 21 GHz are $S_{11} = -3.15\angle -159.8$, $S_{22} = -9.18\angle -149.1$, $S_{21} = -7.40\angle 58.0$, $R_n = 7.965$, $NF_{\text{min}} = 0.762$ and $\Gamma_{\text{opt}} = 0.514\angle 91.037$. The size of the chip transistor is $0.63 \times 0.37 \times 0.1$ mm which works only at 25°C temperature. The circuit design was based on the S2P parameters and noise parameters issued by the foundry. Here, out of the four biasing techniques we opted this circuit so that dc should come to the gate and RF should not enter into the dc. Two power supply is used one is positive and other one is negative to prevent the burn out of GaAs pHEMT Fig. 3 depicts the biasing circuit which was used in this designing to get a good Q point.

To achieve the optimum performance in a microwave amplifier proper input and output matching is required which is obtained using smith chart . The first step in designing of LNA was stability check of the device. The stability can be verified by k and $|\Delta|$ which is mathematically shown below:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} S_{21}|}$$

$$\Delta = S_{11} S_{22} - S_{12} S_{21}$$

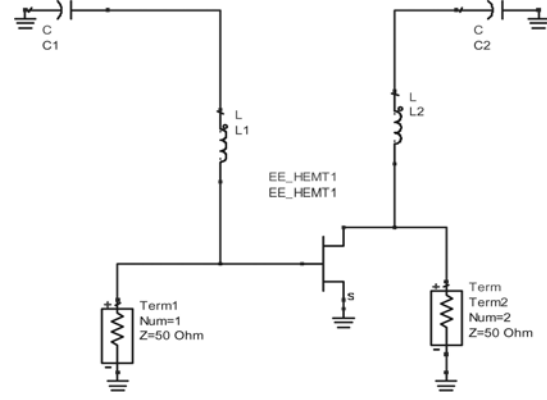


Fig. 3. Biasing circuit of LNA.

The condition for unconditionally stable device is $K > 1$ and $|\Delta| < 1$. In this case, pHEMT transistor is stable as its showing $K > 1$.

Constant gain and noise circles have been drawn to find a valid point on smith chart for reflection coefficients Γ_s so that we have acceptable gain and noise figure values in and out are calculated using formulas 1 and 2.

$$\Gamma_{\text{in}} = \frac{S_{11} + S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L}$$

$$\Gamma_{\text{out}} = \frac{S_{22} + S_{12} S_{21} \Gamma_s}{1 - S_{11} \Gamma_s}$$

III. Simulations and Result

The designing of matching network has been done by choosing proper point on the desired noise figure and gain values. ADS software is used for designing of LNA using RT- duroid substrate having $\epsilon_r = 2.2$, thickness = 0.251mm and loss tangent = 0.0009 for lower losses. The matching network is designed on smith chart using smith utility tool and are shown in Fig. 4 and Fig. 5. Here the lengths and widths for the short circuit stub and microstrip line of the matching networks are calculated using line calc tool.

The input and output return loss at 21GHz is -27dB and -15dB respectively as shown in Fig. 6 and Fig 7. The noise figure of 1.14dB and gain of 25dB of 3 stage LNA from 20 GHz to 22GHz range are shown in Fig 8 and Fig 9. A layout diagram of the 3 stage LNA is given in Fig.10 shown below.

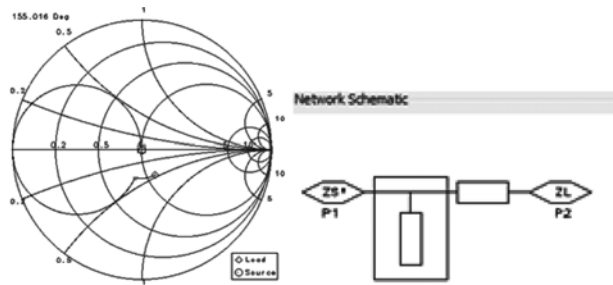


Fig. 4. Smith chart and schematic diagram of Output Matching Circuit.

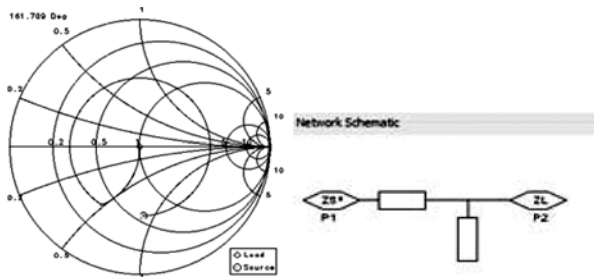


Fig. 5. Smith chart and schematic diagram of Input Matching Circuit.

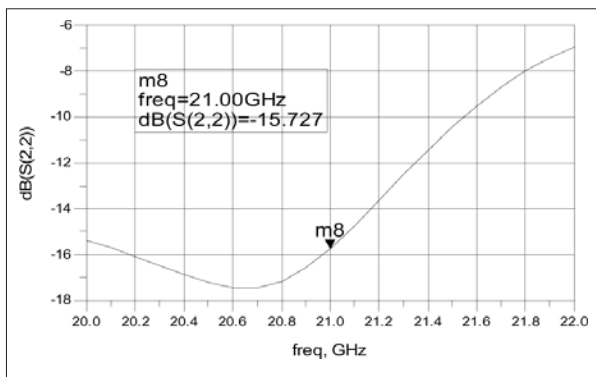


Fig. 6. Graph showing S_{22} of pHEMT LNA

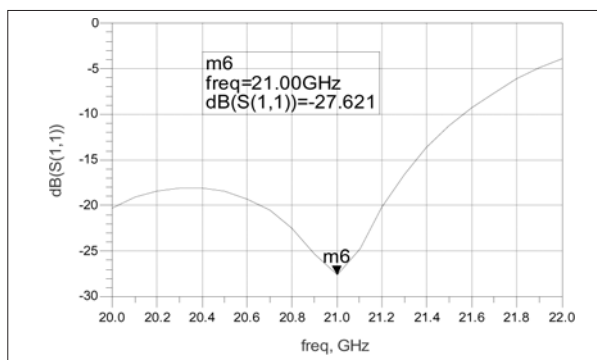


Fig. 7. Graph showing S_{11} of pHEMT LNA

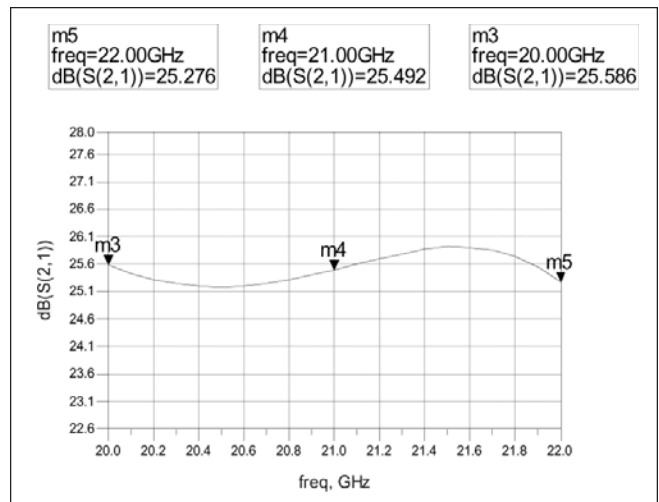


Fig. 8. Graph showing gain S_{21} of pHEMT LNA

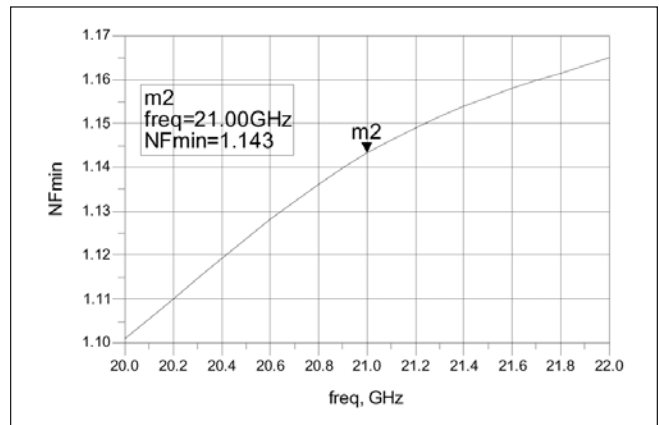


Fig. 9. Graph showing NF_{min} of pHEMT LNA

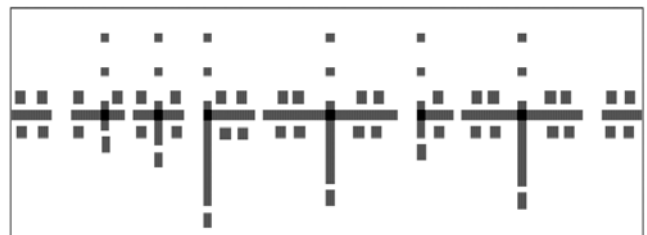


Fig. 10. Layout of 3 Stage LNA

The table1 lists the comparison of this amplifier to other pHEMT LNA at different frequency. From this comparison, the best result for noise figure is reported by this pHEMT LNA design.

Table 1. Comparison of Different Transistors

TRANSISTOR	FREQ	S_{21}	S_{11}	S_{22}	NF_{MIN}	κ
SKY65048	2.5	15-25	-18	-11	0.7	>1
EC2612	21	25.475	-27	-15	1.14	>1
MGA-665P8	4.2	16	-21	-23	1.38	>1
NE76000	5.3	15	-22	-32	1.26	>1
WIN Semiconductor	19	11	-22	-12	3.6	>1

IV. Conclusion

In this paper, the design method of 21Ghz 3 Stage low noise amplifier based on pHEMT technology has been demonstrated. GaAs gated pHEMT with good dc, low noise performance and high uniformity has the minimum noise figure, which can be as low as 1.14dB with an associated gain of 25dB . Furthermore, very good thermal stability for noise performance and associated gain can be seen. As the results show, InGaP/ InGaAs/GaAs pHEMTs are promising for MIC applications that require excellent uniformity and good thermal stability. The design is under fabrication for further development .

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