Stress Generation Techniques in Advanced CMOS

Abstract: *Process-induced strained silicon device technology is being adopted by the semiconductor industry to enhance the performance of the devices in the nanometer realm. The prime area of research is to explore different ways to maximize the desirable strain in the device channel. Difficulties also exist with scaling strain to future technology generations. The stress is a function of different parameters like geometry of the structure, boundary conditions, material parameters, process flow, etc. In this paper, the understanding and issues of MOSFET performance enhancement using strained silicon devices will be discussed. Various processes of strain induction will be reviewed with uniaxial and biaxial stress induction techniques. A range of issues such as stress dependence on critical dimension scaling, effect of buffer layer and silicides etc. are required to be given consideration. At last, the advanced strained silicon on insulator (SSOI) device will be considered as a case of technological importance.*

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I. INTRODUCTION

For the past four decades, geometrical scaling of the transistor dimensions-Moore's Law has dominated the semiconductor industry for greater transistor density and the corresponding transistor performance enhancement. The basic proposal by Dr. Gordon E. Moore was that transistor density on an integrated circuit will approximately double every two years. The switching speed of an ideal transistor can be increased primarily by two ways: physical gate length scaling and carrier mobility enhancement. Strained silicon is a technology, which increases the switching speed solely by enhancing the carrier mobility. In the nanometer regime, biaxial stress has been the conventional method to strain the MOSFET channel. Recent studies in the field of uniaxial process-induced strain have revealed significant advantages over its biaxial counterpart. In this paper, the methods to induce both the types of strain in the MOSFET channel will be discussed.

II. TYPES OF PROCESS INDUCED STRESSES

The residual stresses present in thin films after deposition can be classified into two parts: 1) Thermal mismatch stress and 2) Intrinsic stress. Residual stresses will cause device failure due to instability and buckling if the deposition process is not controlled properly. These different types of process induced stress will now be discussed that are thermal mismatch stress, intrinsic stress and dopant induced stress.

a) *Thermal Mismatch Stress*

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand/contract at different rates. During thermal processing, thin film materials like polysilicon, SiO2, silicon nitride expand and contract at different rates compared to the silicon substrate according to their thermal expansion coefficients. The thermal expansion coefficient, áT, is defined as the rate of change of strain with temperature. Its unit is microstrain/Kelvin (με/K).

b) *Intrinsic Stress*

Intrinsic stress is a type of residual stress, generated due to factors such as deposition rate, thickness and temperature. During deposition, thin films are either "stretched" or "compressed" to fit the substrate on which they are deposited. After deposition, the film wants to be "smaller" if it was "stretched" earlier, thus creating tensile intrinsic stress, and similarly compressive intrinsic stress if it was "compressed" during deposition. This process is illustrated through fig. 1 where the lattice contraction and expansion for boron and germanium atoms doped into silicon substrate are shown [1].

c) *Dopant Induced Stress*

When a dopant atom is introduced in silicon substrate through ion implantation or diffusion, a local

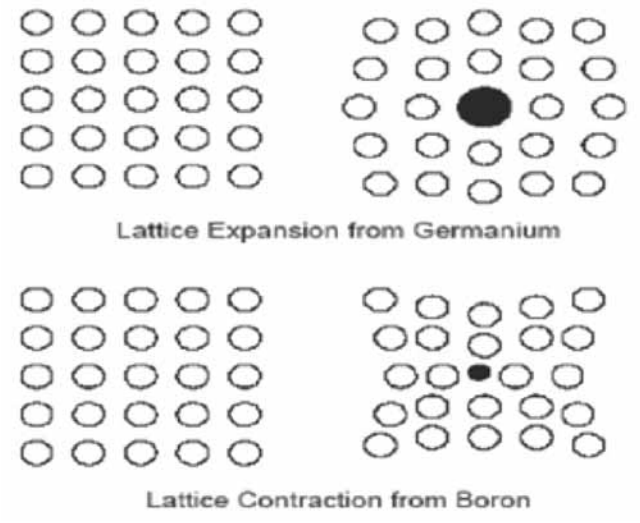

Fig. 1: The Lattice Contraction and Expansion for Boron and Germanium Atoms Doped into Silicon Substrate[1].

lattice expansion or contraction will occur depending on the varying atomic sizes and bond lengths of the atoms [1].

III. BIAXIAL STRESS GENERATION TECHNIQUE

A widely adopted method to introduce wafer-based biaxial stress to enhance CMOS performance is practiced by growing a silicon film atop relaxed SiGe virtual substrate. Due to the lattice mismatch between Si and Ge atoms, tensile biaxial stress is generated in Si film, which enhances the performance of NMOS and PMOS. It can be seen from the piezoresistance coefficients of Si for standard layout and wafer orientation, that NMOS performance (electron mobility) is enhanced by uniaxial longitudinal tensile and out-of-plane compressive stress (fig. 2), while PMOS performance (hole mobility) is enhanced by uniaxial longitudinal compressive stress. Interestingly, both NMOS and PMOS performance is enhanced by biaxial tensile stress.

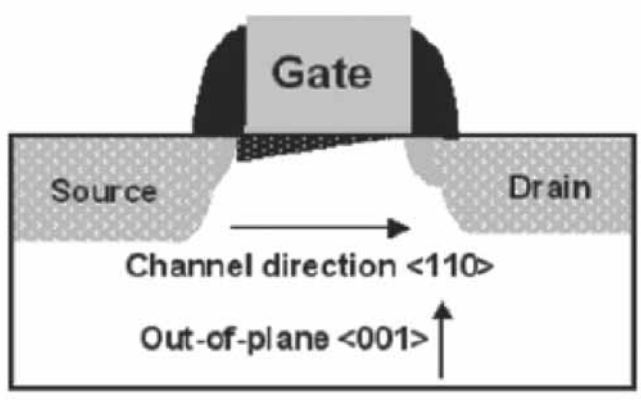

Fig. 2: MOSFET Schematic Device Cross-Section (standard layout)

When a silicon film is deposited on SiGe buffer layer, the film is forced to adopt the greater lattice constant of the SiGe, hence the Si film is under biaxial (longitudinal and transverse) tension, whereas it exhibits an out-of-plane compressive component. This effect is well illustrated in fig. 3 and fig. 4. Fig. 4 illustrates the longitudinal and transverse tensile stress components in the silicon channel on graded SiGe layer.

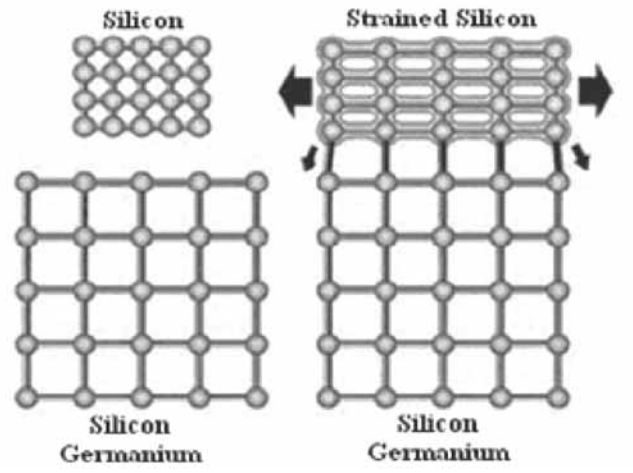

Fig. 3: Steps in Creating Biaxial Strained Si Film Atop SiGe Layer

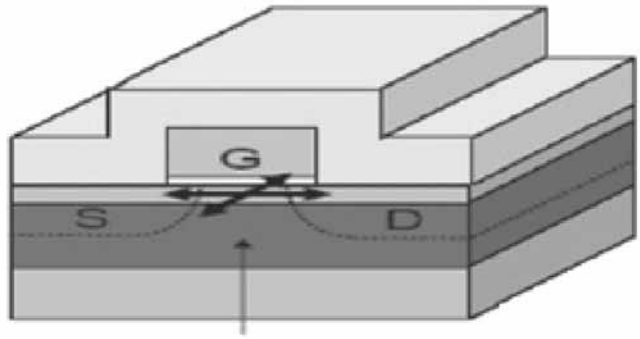

Fig. 4: The Traditional Approach of Generating Biaxial Tensile Stress in MOSFET Channel to Enhance Device Performance [2].

IV. UNIAXIAL STRESS GENERATION TECHNIQUE

Uniaxial process strained silicon is being adopted in nearly all high-performance logic technologies [3]. Channel stress is investigated by introducing a tensile nitride capping layer on the device structure [4]. As a result, the channel stress dependent on the polysilicon

gate and spacer dimensions. A predominant method of introducing uniaxial longitudinal tensile stress is by deposition of CVD silicon nitride film on the device structure. This enhances electron mobility, thereby improving NMOS performance. IBM incorporates compressive silicon nitride capping layer to generate uniaxial longitudinal compressive stress in PMOS channel. With the state-of-the-art processing technology, up to 1.4 GPa process induced tensile stress is generated inside SiN film for NMOS while up to 3.0 GPa compressive stress has been exhibited for PMOS [5].

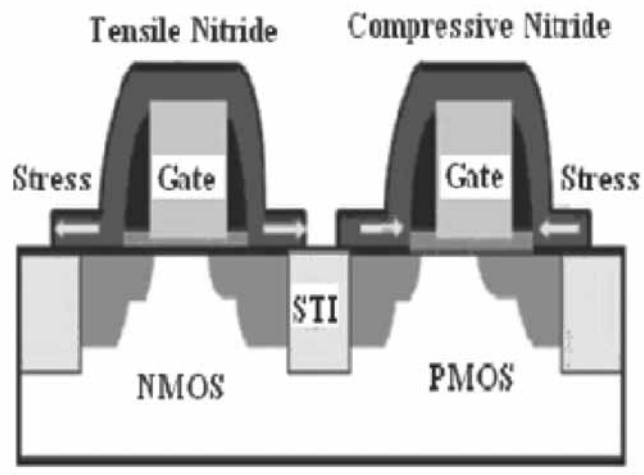

Fig. 5: IBM Technology to Introduce Uniaxial Longitudinal Stress in CMOS Devices [6]

Dual stress linear process architecture with tensile and compressive silicon nitride capping layers is shown in fig.5 over NMOS and PMOS respectively. Similarly, Intel's technology also implements tensile Si3N4 (silicon nitride) capping for n–channel devices. The p-channel device performance is enhanced by using selective SiGe layer as source/drain regions (fig. 6). The lattice

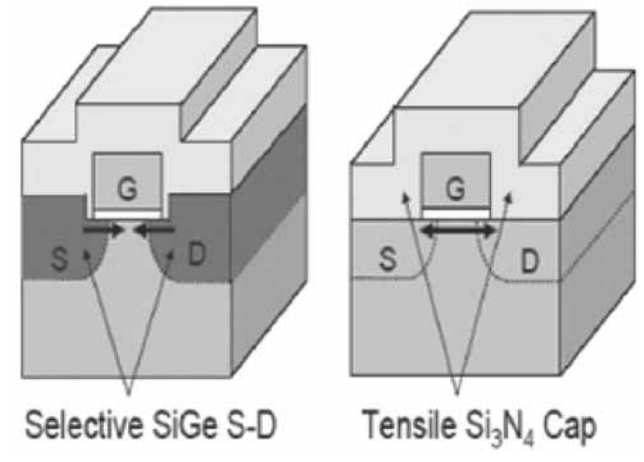

Fig. 6: Intel's Strained Silicon Technology [2]

mismatch in the heterolayer compresses the silicon lattice, which consequently compresses the device channel. For 17% Ge concentration, a compressive stress of 1.4 GPa is generated inside the SiGe layer [5].

V. EFFECT OF VARYING GEOMETRICAL PARAMETER

The effect of varying geometrical parameters on channel stress and thereby on carrier mobility has been an interesting research topic in strained-silicon nanoscale devices.

a) *Critical Dimension Scaling*

The most important parameter that scales with each technology generation is the critical dimension of the physical gate. The channel stress increases as the gate length is scaled since the channel is in closer proximity of the tensile capping Si3N4 layer for smaller critical dimensions.

It can be seen that for oxide spacers, the channel stress is lower than for the nitride spacers because tensile nitride cap relaxes as it pushes against the softer oxide spacers while balancing the forces. This causes lower stress to be transferred into the channel. The nitride film is able to transfer stress to the channel because an edge-force is developed as the film goes over the spacer and gate geometry [7]. An important observation from the results is that it is difficult to strain long- channel devices compared to their short-channel counterparts using tensile nitride capping layer. This is an important consideration the circuit designer should take into account while designing for optimum circuit performance.

b) *Polysilicon Gate Scaling*

With every technology node, the aspect ratio (ratio of length to height) of the polysilicon gate has increased since thicker gates yield higher channel stress for n-channel MOSFETs. Increasing the aspect ratio initially assists in boosting the stress transferred into the device channel from tensile nitride cap, but beyond 150 nm gate thickness, the stress rolls off and remains unchanged. It can be concluded that increasing gate thickness beyond this value only increases the process complexity and deteriorates device performance due to problems like fringing fields. The current 90-nm

technology devices have a gate thickness of 100-140 nm.

c) *Effect of Buffer Layer on NMOS Channel Stress*

A common practice to reduce the font-end process generated defects is to use an unstressed thin silicon nitride buffer film over the structure. This buffer (liner) film, if not properly deposited, proves to be detrimental to the channel stress in NMOS. The tensile nitride capping layer needs to be in close proximity to the substrate (ideally directly onto the substrate) to stress the device channel. The reduction in longitudinal stress upon increasing the liner thickness is generally noticed. Similarly, the out-of-plane compressive stress component, which is also significant in improving n-channel device performance, is reduced upon depositing thicker liner layers.

d) *Effect of Salicide*

Salicides are essential for good contacts with the device terminals. Since salicides are of different material than silicon, it is worth exploring the effect of salicides on the channel stress. Modern process technologies have nickel salicide (NiSi) for the contacts whereas formerly, cobalt salicide (CoSi) was used. Both the salicides have the same material properties (Young's modulus = 161 GPa, Poisson ratio = 0.33) [8, 9]. Salicide thickness can range from 50 °A – 200 °A. Since the salicide has material properties almost same as that of silicon, its presence does not make any significant effect on the stress introduced into the channel.

VI. STRAINED-SILICON-ON-INSULATOR (SSOI)

A large amount of research is being conducted in exploring the possibility of including biaxial strained-Si in mainstream CMOS process to enhance device performance [12]. A novel approach in this direction is to fabricate ultra- thin strained-Si layer on SOI, called strained-silicon-on- insulator (SSOI) [13], thereby complementing their individual advantages. At the future advanced process nodes of 65 nm and below, performance and power consumption issues arise due to bulk silicon's higher leakage currents. SSOI technology has proven thus far to be a promising variation to deal with these issues. The process complexity of fabricating SSOI structure involves transferring a strained-Si/relaxed SiGe hetero-layer on a handle wafer, followed by selective etch- back of SiGe to leave SSOI structure [14]. A homogeneous stress of 1.5 GPa has been exhibited by Soitec Group's [14] industrially manufactured SSOI wafers with a 200 °A Si layer (Fig. 7).

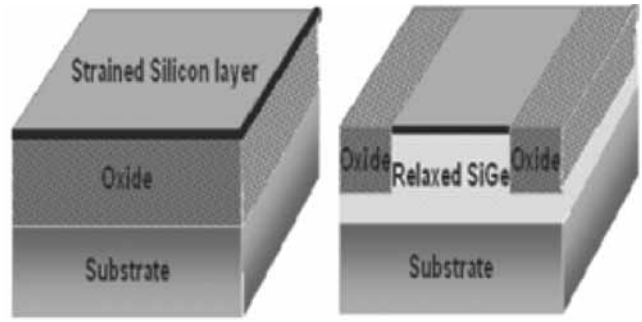

Fig. 7: Stress Relaxation in 200 °A Strained-Silicon on Insulator and on SiGe for different Island Sizes.

The matter of concern in this technology is the stress relaxation due to generation of free surface while forming STI trenches (shallow trench isolation), which leads to wasted active area along the channel width. Consequently, this increases the actual required transistor width than estimated, if the stress relaxation is not accounted for.

Adding to this issue, it can be derived that there is a significant relaxation in the biaxial stress when the film is on oxide compared to atop a SiGe layer. The reason is much higher Young's modulus of SiGe as compared to oxide. It is seen that there is a significant wastage of silicon before the channel stress approaches a value to give optimum performance enhancement. Also a higher peak stress value is gained quickly for thinner silicon compared to the thicker silicon layers. Therefore, a way out to minimize silicon wastage for optimum mobility enhancement is to fabricate devices on thinner strained-silicon membranes.

VII. SUMMARY

In this paper, the sources of strain in MOSFETs are discussed which is followed by a brief understanding of different types of stresses. Next, the state-of-the-art stress generation techniques, for both wafer-based biaxial and locally-induced uniaxial stresses are discussed. Finally, the effects of scaling different geometrical parameters for n- channel devices are explained. Feature of strained silicon technology is that it increases the switching speed by enhancing the carrier

mobility. If the deposition process is not controlled properly then residual stresses will cause device failure due to instability and buckling. Uniaxial longitudinal tensile and out-of-plane compressive stress are used to enhance electron mobility and hole mobility is enhanced through uniaxial longitudinal compressive stress. Chemical vapour deposition (CVD) method is used for inducing uniaxial longitudinal tensile stress by deposition of silicon nitride film on the device structure. It is found difficult to strain long- channel devices as compared to their short-channel counterparts using tensile nitride capping layer. As material properties of salicide is almost same as that of silicon, its presence does not effect on the stress introduced into the channel significantly. We are giving emphasis on ultra –thin strained-Si layer on SOI, so that advantages of both Stress induction and SOI devices could be incorporated. In SSOI technology, the stress relaxation due to generation of free surface while forming STI (shallow trench isolation) trenches is of major concern. By fabricating devices on thinner strained-silicon membranes silicon wastage could be minimized for optimum mobility enhancement.

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