Comparative Study and Implementation of Vedic Multiplier for Reversible Logic Based ALU

Shaveta Thakral
Research Scholar
ECE Deptt., FET
Manav Rachna International University
Faridabad, India
E-mail: Shaveta.fet@mriu.edu.in

Dipali Bansal
Professor & Head
ECE Deptt., FET
Manav Rachna International University
Faridabad, India
E-mail: dipali.fet@mriu.edu.in

Abstract: ALU is fundamental building block of modern computing environment supported by embedded processors. The demand for low power consumption & high processing speed has been increasing in modern scientific computers and signal processing applications. Speed of ALU depends mainly on multipliers and multipliers are generally slowest in speed. Therefore reversible logic based Vedic Multiplier need to be designed for the implementation of ALU to add on high speed and low power requirements. The main aim of this paper is to present critical review of existing Vedic multipliers The existing Vedic multipliers are coded in Verilog HDL, synthesized and simulated using EDA (Electronic Design Automation) tool-Xilinx ISE design suit 14.2. Finally the results are compared for all existing multipliers in terms of ancillary inputs, garbage outputs, number of reversible logic gates and quantum cost.

Keywords: Vedic multiplier, Reversible logic, ALU, Verilog HDL, Quantum cost

I. INTRODUCTION

(Landauer, 1961) stated that "amount of energy dissipated for every bit erasure during an irreversible operation is given by KTln2 joules where K is Boltzmann's constant, and T is the operating temperature". (Bennett,1973) proposed the solution to Landauer statement and showed that KTln2 energy dissipation would not occur, if computation is done in a reversible manner since amount of energy dissipated in a system depends directly on numbers of bits erased during computation. Classical gates like two input AND, OR, NAND, NOR, XOR and XNOR are irreversible as input states can't be uniquely reconstructed from output states. Here two-bit input state is mapped to one-bit output state leads to the erasure of one bit and consequently loss of energy. This energy loss can be avoided by mapping n bit input states to n bit output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible. Quantum gates or reversible gates differ from Classical gates in a way that a) quantum gates work on qubits rather than bits b) feedbacks are not permitted in reversible logic circuits made with reversible logic gates so called acyclic and c) there is no fan out allowed means several copies of qubits are not allowed. The optimization metrics of reversible logic circuits are quantum cost, ancillary input, garbage output and delay etc. are given below:

The quantum cost of a reversible gate is total number of 1x1 and 2x2 reversible gates required in the design. The quantum costs of all reversible 1x1, as well as 2x2 gates, are taken as one. Since every reversible gate consists of various 1 x 1 or 2 x 2 quantum gates are taken from NCV gate library containing combinations of NOT, CNOT and controlled V and controlled V+ gates, therefore the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V+ and CNOT gates. Integrated qubit gates are also used in the quantum implementation of reversible logic gates. Integrated qubits are a combination of Feynman gate and either controlled V or controlled V+ gate. Quantum cost of integrated qubit gate is also one Quantum cost for any reversible logic circuit should be as low as possible.

To achieve reversibility, It is must to map n bit input states to bit n output states and sometimes every gate output is not used as input to some other gates nor acting as a useful desired output. These undesired or unused outputs that are deliberately obtained to maintain reversibility criterion of a reversible gate (or circuit) are known as Garbage Outputs. Garbage outputs

for any reversible logic circuit should be as low as possible.

To achieve reversibility, It is must to map n nit input states to n bit output states. These constant inputs 0 or 1 which are deliberately applied to maintain reversibility criterion of a reversible gate (or circuit) are known as Ancillary Inputs. Ancillary inputs for any reversible logic circuit should be as low as possible.

The maximum number of gates in a path from any input line to any output line in any reversible logic circuit is called as the delay. Two assumptions need to be considered for calculation of delay: (i) Each gate performs computation in one unit time and (ii) all inputs to the circuit are available before the computation begins. The delay of each 1x1 gate and 2x2 reversible gates is taken as unity. Delay for any reversible logic circuit should be as low as possible.

II.VEDIC MATHEMATICS BASED MULTIPLIER

Vedic mathematics was constructed by Shri Bharati theertazi (1884-1960). This mathematics contains 16 main sutras and 16 sub sutras. Vedic mathematics reduces efforts of complex mathematical calculations. The proposed multiplier is based on Urdhva Tiryagbhyam sutra which means "Vertically and crosswise". "Urdhva Tiryagbhyam" Sutras are applied here on binary numbers for multiplication. The algorithm can handle n x n bit multiplication by breaking it into smaller sizes. Generation of all partial products in vedic multiplier can be done with the concurrent addition of partial products. 2*2 is considered to be basic block which is implemented using two half adder modules as shown in Fig.1.The circuit of Vedic multiplier consist of 6 AND and 2 XOR gates as shown in Fig.2.The method for Vedic multiplication of 2 bit binary numbers is illustrated in Fig.3.The implementation equations of 2*2 Vedic multiplier are: P0 = a0b0, P1= a1b0 ⊕a0b1, C1 = (a1b0). (a0b1), P2 = a1b1 ⊕ C1, P3 = (a1b1).C1

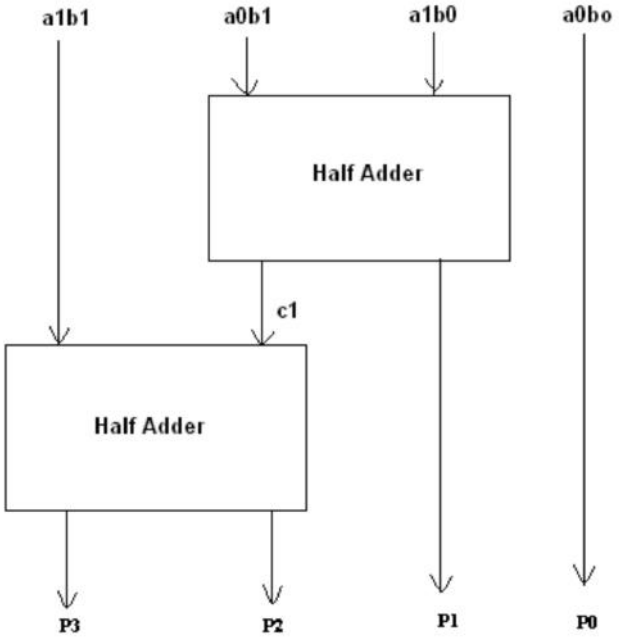

Fig.1: Block diagram of 2*2 vedic multiplier

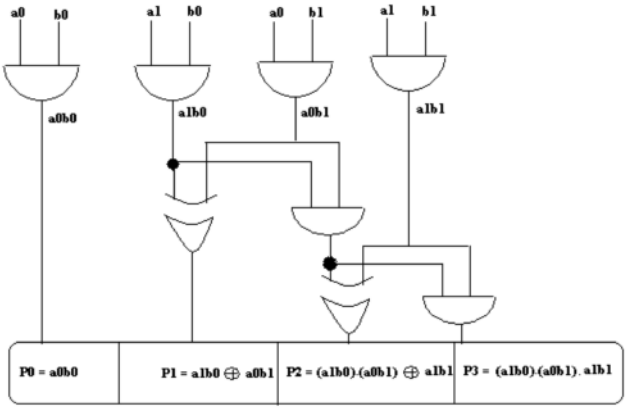

Fig. 2: Circuit Diagram of 2*2 vedic multiplier

III. EXISTING VEDIC MULTIPLIERS

Reversible logic gates used in existing vedic multiplier are given in section a . Existing vedic multiplier designs are given in section b. Table1-6 illustrates their specification, expression, quantum cost and feature.

A) Reversible logic gates used for vedic multipliers

Table 1: Toffoli Gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
Toffoli/CCNOT Gate	3*3	P = A Q = B R = AB⊕C	5	Universal Reversible Logic Gate

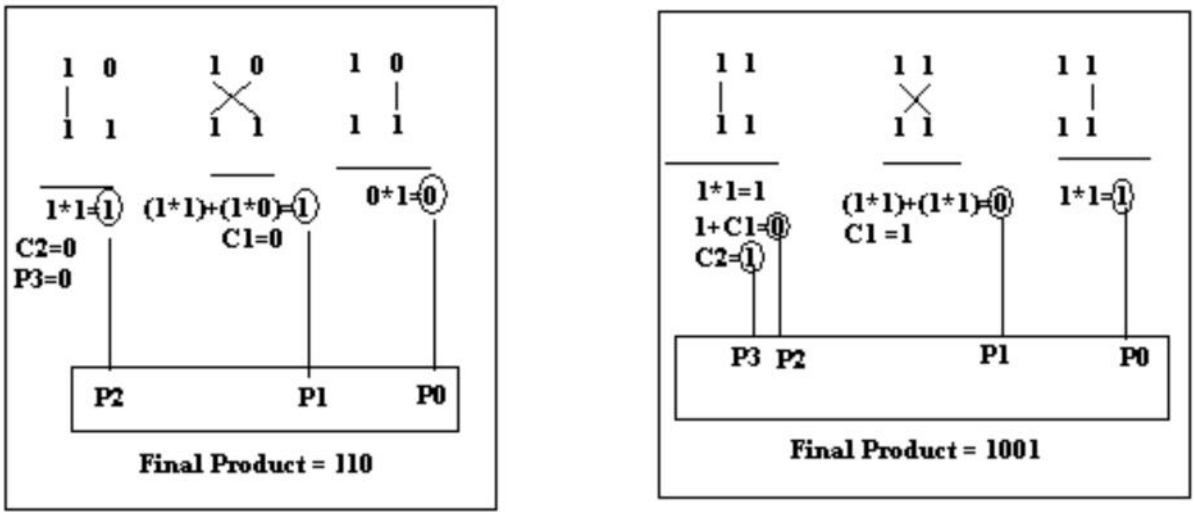

Fig. 3: Method for Vedic multiplication

Table 2: Peres Gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
Peres Gate/NTG	3*3	P = A Q = A ⊕ B R = AB ⊕ C	4	Lowest Quantum Cost

Table 3: CNOT Gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
CNOT Gate/ Feynman Gate	**2*2**	P = A Q = A ⊕ B	**1**	**Copying gate, Fanout Gate**

Table 4: NFT Gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
NFT Gate	3*3	P = A ⊕ B Q = B$\overline{C}$ ⊕ A$\overline{C}$	5	Parity Preserving Gate

Table 5:. BVPPG gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
BVPPG Gate	5*5	P = A Q = B R = AB ⊕ C S = D T = AD ⊕ E	10	Partial Product Generator

Table 6: BME gate

Reversible Logic Gate	*Specification*	*Expression*	*Quantum Cost*	*Feature*
BME Gate	4*4	P = A Q = AB ⊕ C R = AD ⊕ C S = AB ⊕ C ⊕ D	6	Partial Product Generator

B. Existing Designs

Researchers have proposed several methodologies to convert irreversible logic based vedic multiplier into reversible logic based multiplier to save power .Various existing designs are given here.

(Sharma et al. 2014) proposed design1 using four toffoli gates and two peres gate. Circuit diagram is shown in Fig.4 and simulation waveform is shown in Fig.5. Proposed circuit took six ancillary inputs, produced six garbage outputs. Quantum cost of proposed circuit is 28. Optimization metrics are given in Table 7.

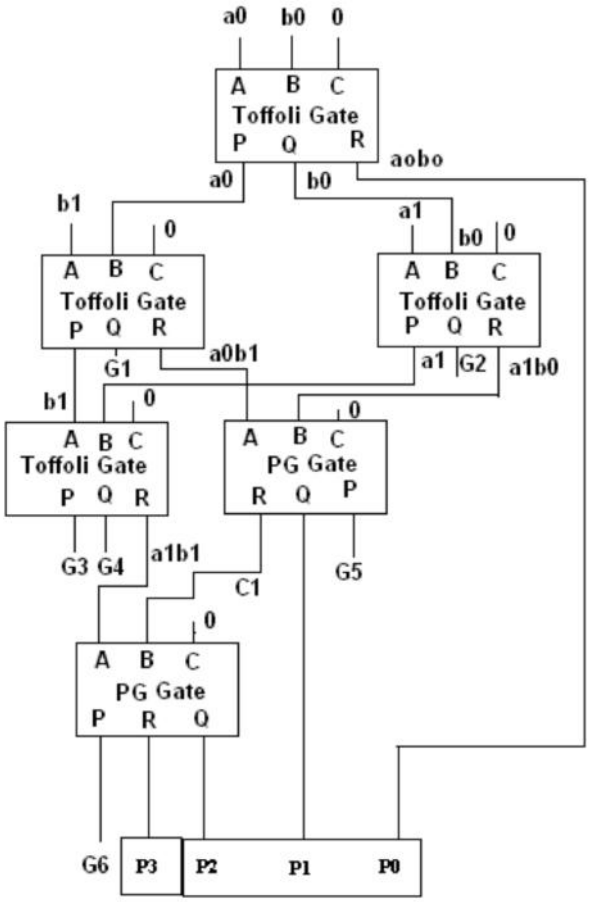

Fig. 4: Existing Design 1

Table 7: Optimization Metrics: Design 1

Garbage outputs	6
Ancillary inputs	6
Quantum Cost	28
Number of Gates	6

(Rakshith and Saligram,2013) proposed design2 using five peres gates and one CNOT gate (Feynman gate).Circuit diagram is shown in Fig.6 and simulation waveform is shown in Fig. 7. Proposed circuit took four ancillary inputs, nine garbage outputs. Quantum cost of proposed circuit is 21. Major drawback of this design is that it suffers from fan out problem yet it is not permitted in reversible logic circuits. Optimization metrics are given in Table 8.

Table 8: Optimization Metrics: Design 2

Garbage outputs	9
Ancillary inputs	4
Quantum Cost	21
Number of Gates	6

(Rakshith and Saligram, 2013) proposed improved design3 using one BVPG gate, three peres gates and one CNOT gate (Feynman gate). Circuit diagram is shown in Fig. 8 and simulation waveform is shown in Fig. 9. Proposed circuit took five ancillary inputs, five garbage outputs. Quantum cost of proposed circuit is 23. This design overcomes fan out drawback suffered by design 2. Optimization metrics are given in Table 9.

Table 9: Optimization Metrics: Design 3

Garbage outputs	5
Ancillary inputs	5
Quantum Cost	23
Number of Gates	5

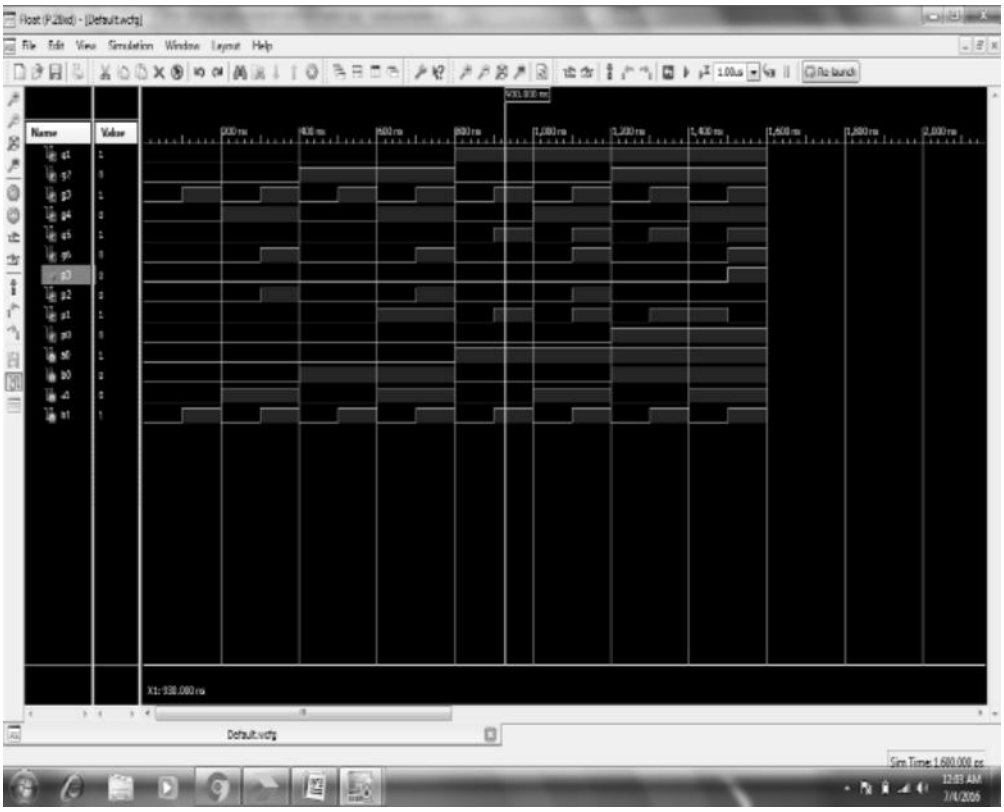

Fig. 5: Simulation Waveform: Existing Design 1

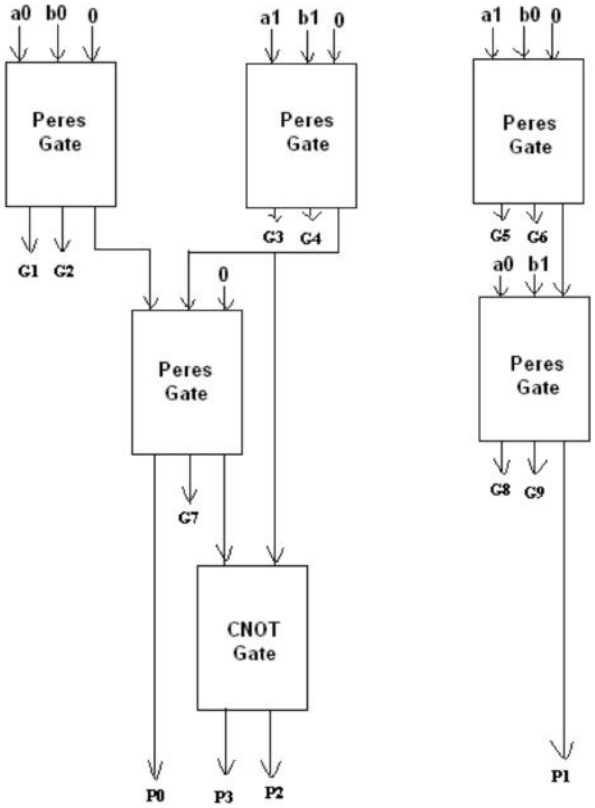

Fig. 6: Existing Design 2

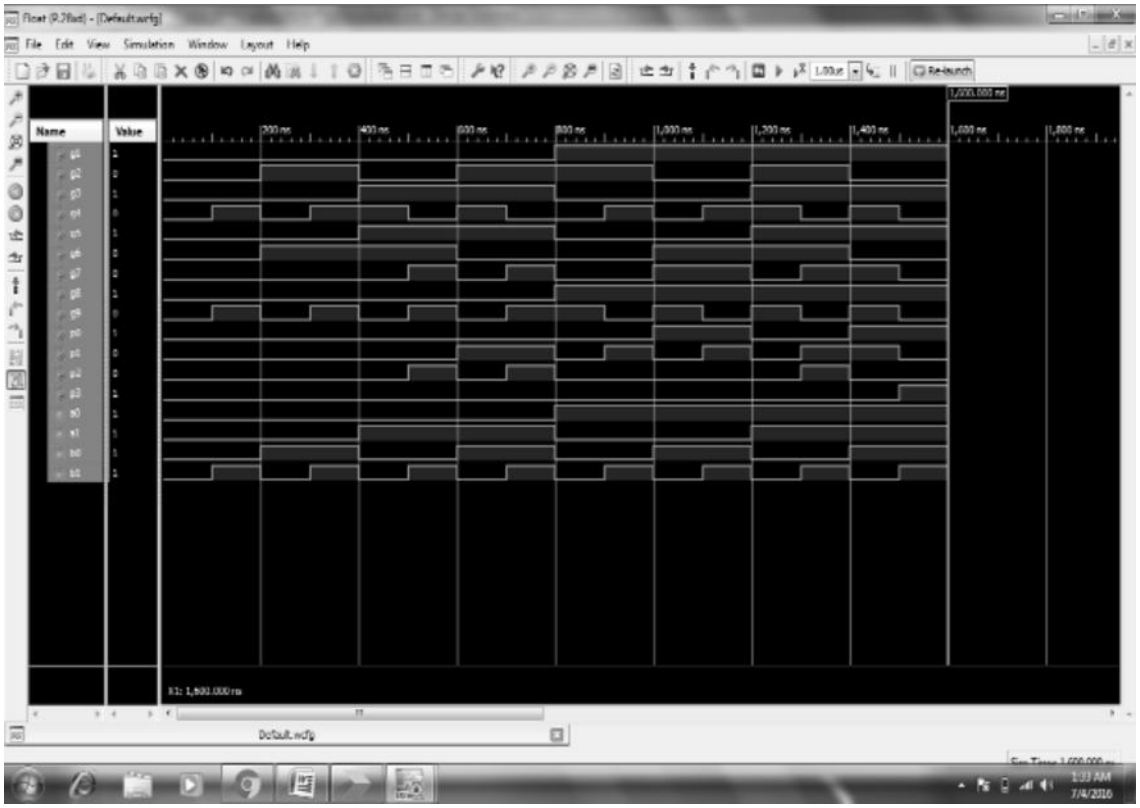

Fig. 7: Simulation Waveform: Existing Design 2

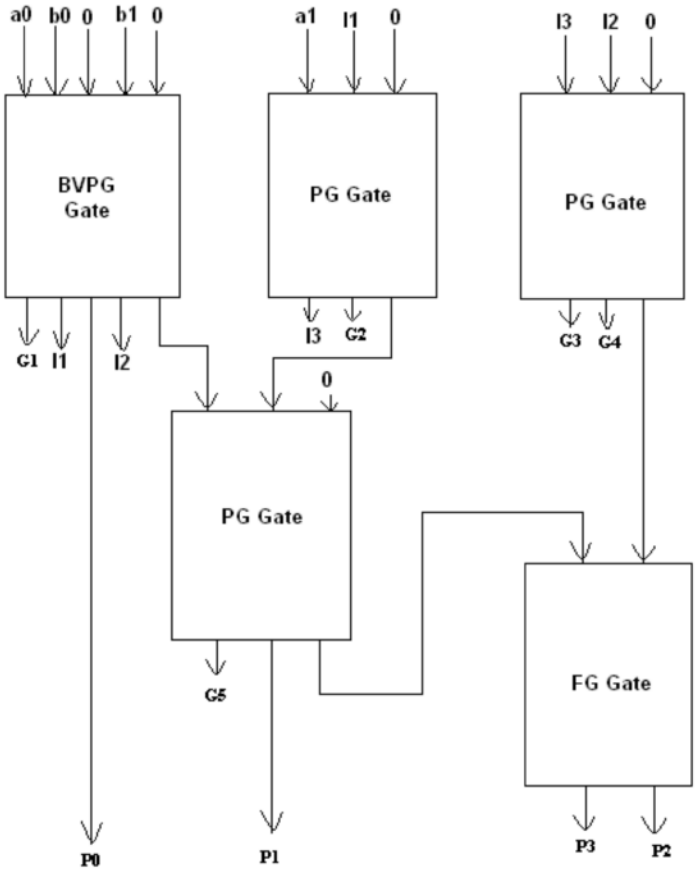

Fig. 8: Existing Design 3

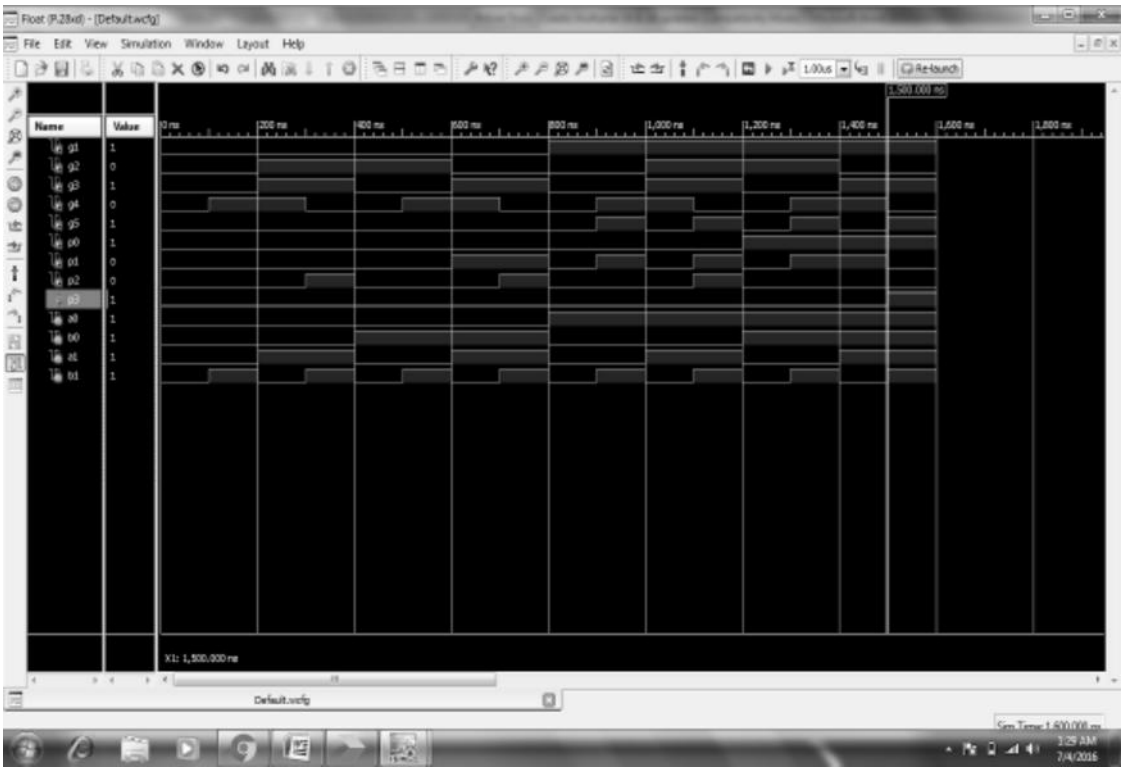

Fig. 9: Simulation waveform: Existing Design3

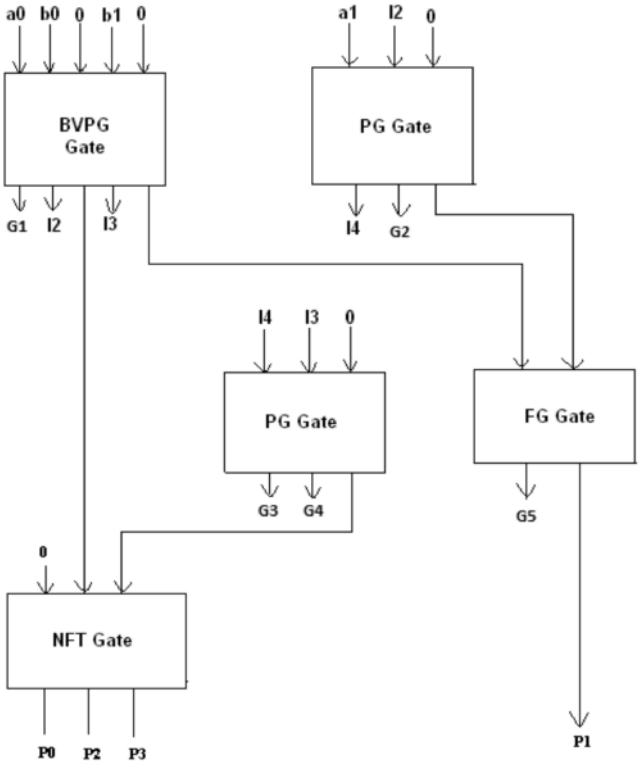

Fig. 10: Existing Design 4

Rakshith and Saligram, (2013) proposed one more improved design4 over design 2 using one BVPG gate, two peres gates, one NFT gate and one CNOT gate (Feynman gate).Circuit diagram is shown in Fig.10 and simulation waveform is shown in Fig.11. Proposed circuit took six ancillary inputs, four garbage outputs. Quantum cost of proposed circuit is 24. This design also overcomes fan out drawback suffered by design 2. Optimization metrics are given in Table 10.

Table 10: Optimization Metrics: Design 4

Garbage outputs	5
Ancillary inputs	6
Quantum Cost	24
Number of Gates	5

Shivarathnamma, (2016) proposed design 5 using one BME gate, three peres gates and one Toffoli gate. Circuit diagram is shown in Fig.12 and simulation waveform is shown in Fig.13. Proposed circuit took five ancillary inputs and produced seven garbage outputs. Quantum cost of proposed circuit is 23.This design also overcomes fan out drawback suffered by design 2. Optimization metrics are given in Table 11.

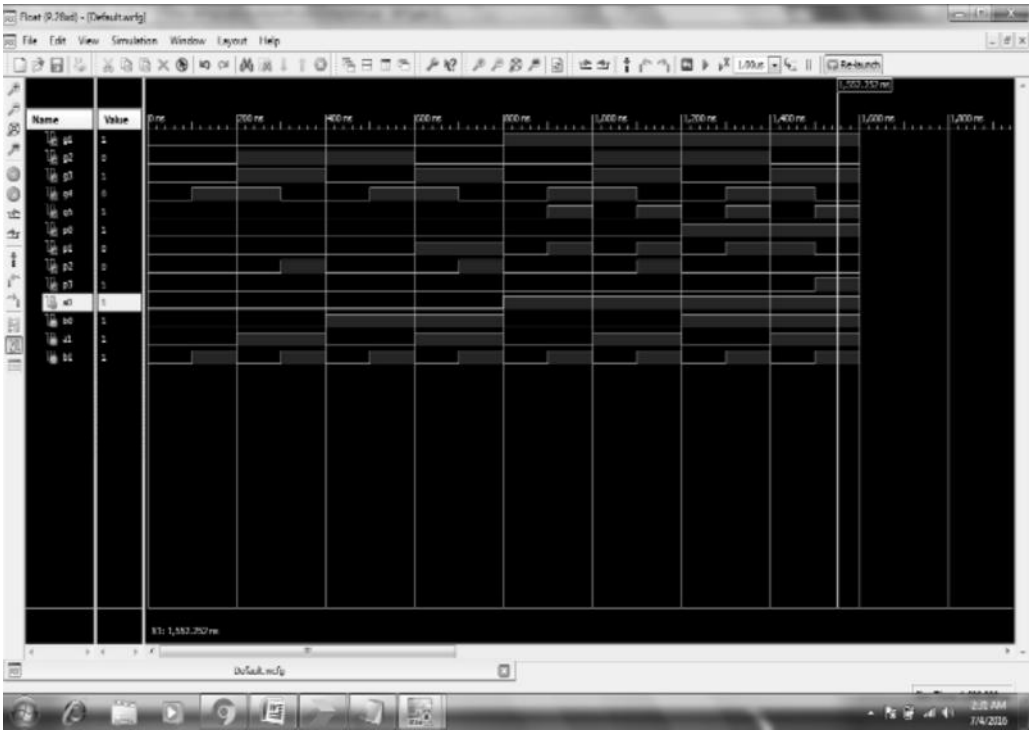

Fig. 11: Simulation Waveform: Existing Design 4

Table 11: Optimization metrics: Design 5

Garbage outputs	7
Ancillary inputs	5
Quantum Cost	23
Number of Gates	5

IV. COMPARISON OF VARIOUS EXISTING DESIGNS

The existing designs are compared in terms of various optimization metrics like ancillary inputs, garbage outputs, quantum cost and number of reversible logic gates used. Optimization metrics comparison is given in Table 12. Comparative analysis is shown in Fig. 14. Although design2 has least quantum cost yet it suffers from fan out problem and not found to be suitable for reversible logic implementation. Design 3 and design 5 are found be be with same quantum cost yet design 3 produces less garbage. Hence it is considered to be most optimum design among existing designs.

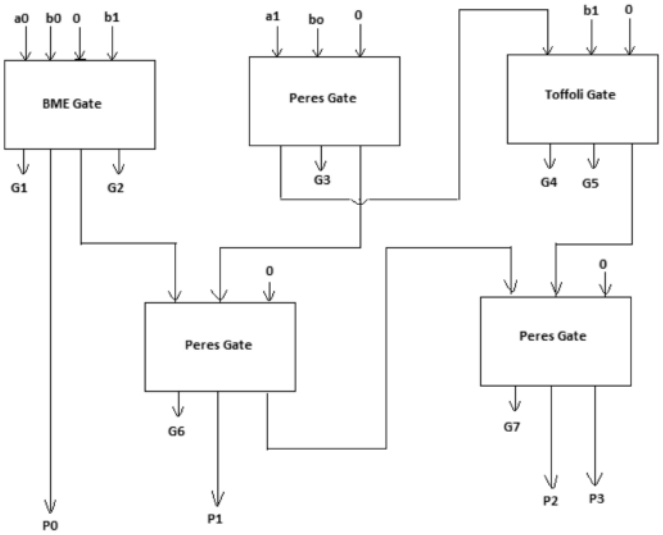

Fig. 12: Existing Design 5

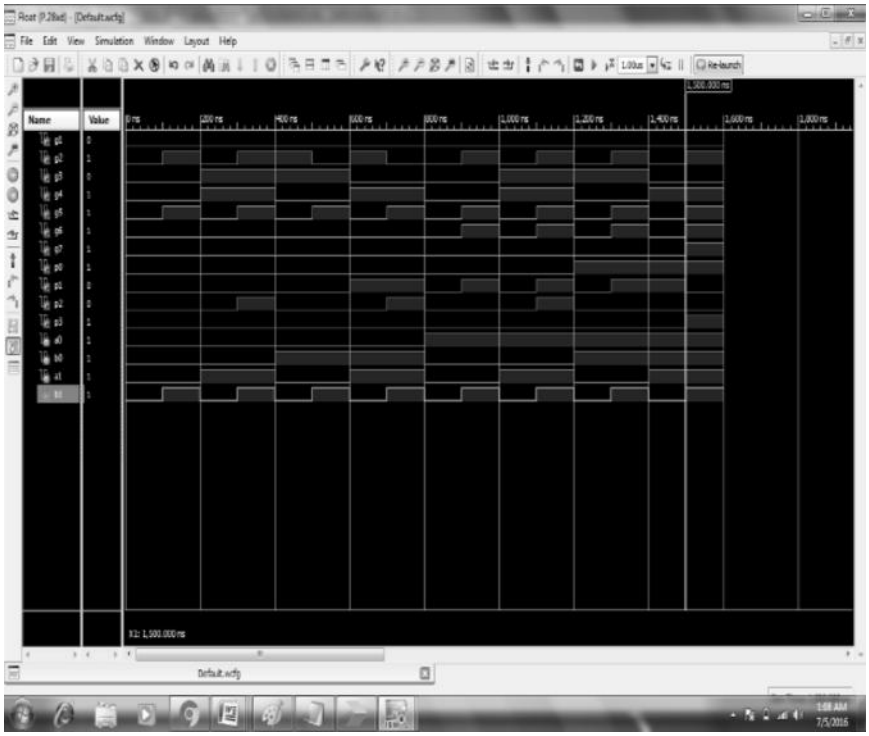

Fig. 13: Simulation Waveform: Existing Design 4

V. CONCLUSION

The main aim of this paper is to present critical review of Vedic multipliers. The existing Vedic multipliers are coded in Verilog HDL, synthesized and simulated using EDA (Electronic Design Automation) tool-Xilinx ISE design suit 14.2. Finally comparative analysis is done for all existing multipliers in terms of ancillary inputs, garbage outputs, number of reversible logic gates and quantum

cost. Future scope is to design low quantum cost reversible logic based Vedic Multiplier for implementation of ALU to add on high speed and low power requirements.

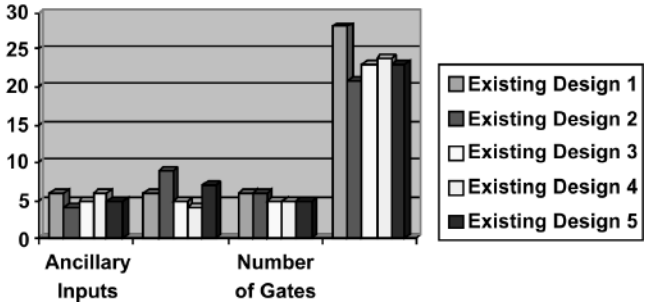

Fig. 14: Comparative Analysis of Existing Vedic Multiplier Designs

Table 12: Optimization Metrics Comparison of Existing Vedic Multiplier Designs

Vedic Multiplier	Ancillary Inputs	Garbage Outputs	Number of gates	Quantum Cost
Existing Design1	6	6	6	28
Existing Design2	4	9	6	21
Existing Design3	5	5	5	23
Existing Design4	6	5	5	24
Existing Design5	5	7	5	23
Best findings	Existing Design 2	Existing Design 3,4	Existing Design 3,4,5	Existing Design 2

REFERENCES

[1] Bassi, M., Verma, S. and Kaur, R., 2016. Design of an efficient low power multiplier: Combining reversible and an ancient vedic method approach.*Indian Journal of Science and Technology*, *9*(7).

[2] Belayet Ali, M. (2011). Design of Reversible Sequential Circuit Using Reversible Logic Synthesis.*International Journal of VLSI Design & Communication Systems*, 2(4), pp.37-45.

[3] Bennett, C. (1973). Logical Reversibility of Computation. *IBM Journal of Research and Development*, 17(6), pp.525-532.

[4] Biswas, A., Hasan, M., Chowdhury, A. and Hasan Babu, H. (2008). Efficient approaches for designing reversible Binary Coded Decimal adders. *Microelectronics Journal*, 39(12), pp.1693-1703.

[5] Christina, X., Justine, M., Rekha, K., Subha, U. and Sumathi, R. (2010). Realization of BCD adder using ReversibleLogic. *IJCTE*, pp.333-337.

[6] Das, A. and Bha, M.J.K., 2014, January. Design Optimization of Vedic Multiplier using Reversible Logic. In *International Journal of Engineering Research and Technology* (Vol. 3, No. 3 (March-2014)). ESRSA Publications.

[7] Guan, Z., Li, W., Ding, W., Hang, Y. and Ni, L. (2011). An Arithmetic Logic Unit design based on reversible logic gates. In: *Communications, Computers and Signal Processing (PacRim), 2011 IEEE Pacific Rim Conference*. Victoria, BC: IEEE, pp.925-931.

[8] Gupta, A., Malviya, U. and Kapse, V., 2012, December. Design of speed, energy and power efficient reversible logic based vedic ALU for digital processors. In *2012 Nirma University International Conference on Engineering (NUiCONE)* (pp. 1-6). IEEE.

[9] Haghparast, M. and Shoaei, S. (2015). Design of a New Parity Preserving Reversible Full Adder.*Journal of Circuits, Systems and Computers*, 24(01), p.1550006.

[10] Landauer, R. (1961). Irreversibility and Heat Generation in the Computing Process. *IBM Journal of Research and Development*, 5(3), pp.183-191.

[11] Mamataj, S. and Das, B. (2014). Approaches to realize Canonical Form of Boolean Expression by using Reversible COG Gates. *International Journal of Computer Applications*, 92(2), pp.15-21.

[12] Morrison, M., Lewandowski, M., Meana, R. and Ranganathan, N. (2011). Design of a Novel Reversible ALU using an Enhanced Carry LookAhead Adder. In: *11th IEEE International Conference on Nanotechnology*. Portland Marriott: IEEE.

[13] Parween, A.S. and Murugeswari, S., 2014. A Design of High Speed, Area Efficient, Low Power Vedic Multiplier using Reversible Logic Gate.*International Journal of Emerging Technology and Advanced Engineering*,*4*(2).

[14] Peres, A. (1985). Reversible logic and quantum computers. *Phys. Rev. A*, 32(6), pp.3266-3276.

[15] Rakshith, T.R. and Saligram, R., 2013, March. Design of high speed low power multiplier using Reversible logic: A Vedic mathematical approach. In*Circuits, Power and Computing Technologies (ICCPCT), 2013 International Conference on* (pp. 775-781). IEEE.

[16] Saligram, R. and T.R., R. (2012). Novel Code Converter Employing Reversible Logic. *International Journal of Computer Applications*, 52(18), pp.24-29.

[17] Saligram, R. and Rakshith, T.R., 2013, April. Optimized reversible Vedic multipliers for high speed low power operations. In *Information & Communication Technologies (ICT), 2013 IEEE Conference on* (pp. 809-814). IEEE.

[18] Saravanan, P., Chandrasekar, P., Chandran, L., Sriram, N. and Kalpana, P., 2012. Design and implementation of efficient vedic multiplier using reversible logic. In *Progress in VLSI Design and Test* (pp. 364-366). Springer Berlin Heidelberg.

[19] Saravanan, S., Vennila, I. and Mohanram, S., 2016. Design and Implementation of Efficient Reversible Arithmetic and Logic Unit. *Circuits and Systems*, *7*(06), p.630.

[20] Sharma,N., Saraswat,U.,Sachdeva,R. Novel High Speed Low Power Binary Multiplier Designs using Reversible Logic Gates.International Journal of Computer Applications.105(9), pp.9-13

[21] Shivarathnamma, G.J. and Kurian, M.Z., A Novel approach of 4* 4 Vedic Multiplier using Reversible Logic Gates.In 1st International Conference on Innovations in Computing & Networking (ICICN16),pp.538-542

[22] Singh, R., Upadhyay, S., S, S., KB, J. and SA, H. (2014). Efficient Design of Arithmetic Logic Unit using Reversible Logic Gates. *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)*, 3(4), pp.1474-1477.

[23] Syamala, Y. and Tilak, A. (2011). Reversible Arithmetic Logic Unit. In: *Electronics Computer Technology (ICECT), 2011 3rd International Conference*. Kanyakumari: IEEE.

[24] Thomsen, M., Glück, R. and Axelsen, H. (2010). Reversible arithmetic logic unit for quantum arithmetic. *Journal of Physics A: Mathematical and Theoretical*, 43(38), p.382002.

[25] Zhang, K., Fan, W., Deininger, P., Edwards, A., Xu, Z. and Zhu, D. (2009). Breaking the computational barrier: a divide-conquer and aggregate based approach for Alu insertion site characterisation.*International Journal of Computational Biology and Drug Design*, 2(4), p.302.

❐