Comparative Analysis of D Flip Flop using various Submicron Technologies

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Abstract: As technology is getting scale down so delay, power and area perform a critical role in the designing and calculation of numerous digital circuit applications. Portable devices are in demand now a day's hence designing of low power devices is very necessary. So, detail analysis of digital circuits in terms of power, delay, performance, and area is essential. D Flip Flop is one of the important digital circuits which have enormous applications in various digital designs. Hence, this paper presents performance analysis of D Flip flop circuit using various technologies and their comparative analysis in terms of power dissipation and delay. This circuit has been designed using Tanner EDA tool with different technologies (i.e. 45nm, 90nm and 180nm). The power dissipation and delay of 45nm technology is less than the other two technologies.

Keywords—D Flip flop, Complementary Metal Oxide Semiconductor (CMOS), Low power, Transmission Gate (TG) and Tanner Tool.

I. INTRODUCTION

Power dissipation is very necessary consideration and plays a vital role in the design of an IC in the current days of IC technology. Delay and power are two major factors which must be taken into consideration when movable devices are to be designed [1]. In various digital circuits, flip-flops are necessary state holding circuits which have a large effect on delay and power dissipation of system. To find the performance of complete system, it is essential to find the function of a flip-flop. Performance is proportional to clock frequency and the power consumption. In the digital systems 30% to 70% of overall power are observed in the clocking network and Flip-Flops [2].

As the uses of portable devices are increasing, low power consumption is required [3]. So the main purpose of the design is to find the power dissipation of D Flip flop for various technologies. Here, an edge triggered D flip flop is designed and it is compared with various technologies. This D flip flop will be designed on 45 nm, 90 nm and 180 nm technologies.

Flip-Flops are electronic circuits which store 0 or 1 logic depending on the response of the clock with input data [4]**.** D Flip Flop is one of the important digital circuits which have enormous applications in various digital designs [5].

Dissipated power in digital CMOS circuits (P_{TOTAL}) is the addition of three powers, the first is static power, and the second is dynamic power and third is short Circuit power.

$$P_{TOTAL} = P_{SH} + P_{DY} + P_{SC}$$

The leakage powers are most significant. The powerful contributor of power dissipation in CMOS circuits is leakage current as it is higher than others and other components are getting reduced such as threshold voltage component, gate oxide thickness components and channel length components[6].

The theory of D Flip flop and the methodology used is described in section II. Section III shows the desired results in terms of schematics and their waveforms, comparison table of different technologies is also discussed. Section IV concludes the work done in the paper.

II. METHODOLOGY

The D flip-flop is extensively used flip flop in synchronous circuit. D flip flop is also called data flip-flop. The D flip-flop holds data input at a particular fraction of the clock [7]. That obtained value now goes to the Q output. Otherwise the Q output does not switch.

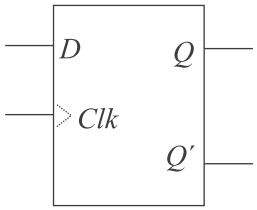

Fig. 1. D Flip-Flop Symbol

The symbol of D flip flop is shown in the figure1 and the truth table is shown in the Table 1.

Table 1 D Flip-Flop Excitation

Q	QNext	D
0	0	0
0	1	1
1	0	0
1	1	1

In many digital circuit applications the D latch is used specially to store the data temporally or used as a delay element [8]. It (Fig. 2) shows the circuit of D flip flop consists of two- inverter connected back to back and two CMOS transmission gate (TG) used as switches. At the input, the clock signal is used to activate transmission gate, and in the loop of inverter the TG is activated by the inverted clock signal [9]. At the time of high pulse of clock, the data input is stored into the circuit and during the low clock input; this stored data is sustained in the form of inverter loop's stage [10].

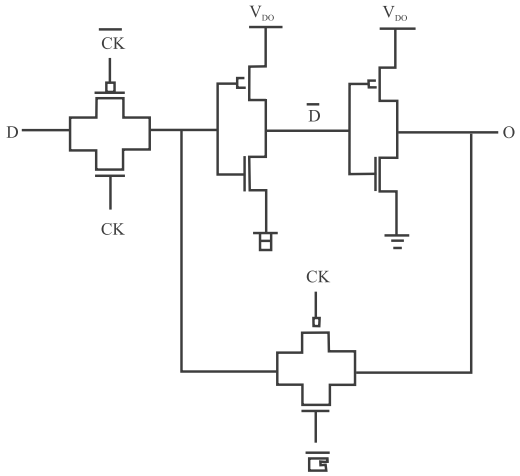

Fig. 2. D Flip flop using transmission gate

III. SIMULATION AND RESULTS

The given system is designed using Tanner tool version 13. The designed system is simulated on 45 nm, 90 nm and 180nm technologies. The Schematic of D flip flop is shown in Fig. 3. Figs. 4, 5 and 6 shows the result of the given D flip flop on different technologies 45nm, 90nm and 180nm respectively.

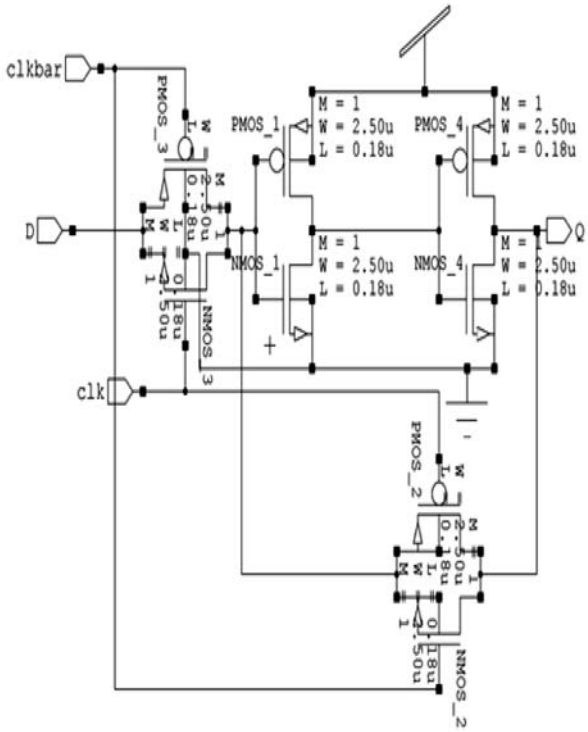

Fig. 3. Schematic of D Flip flop

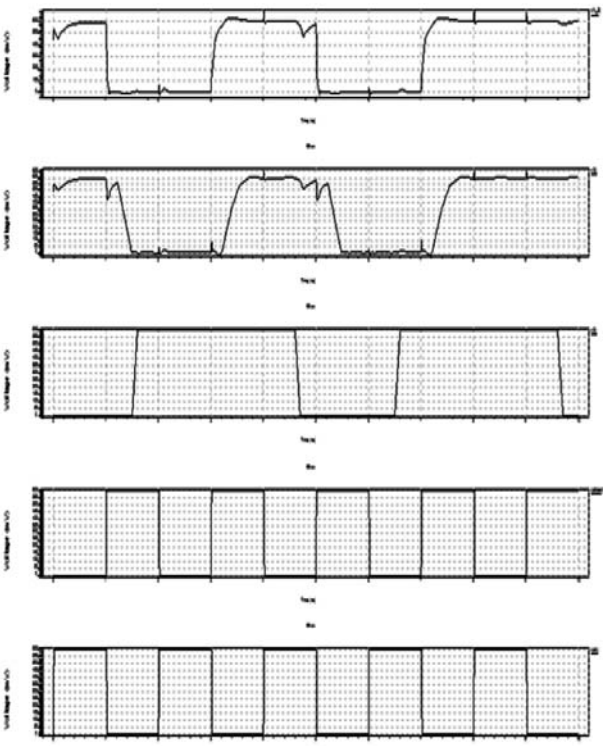

Fig. 4. Waveform of transient analysis of D FF for 45nm Technology

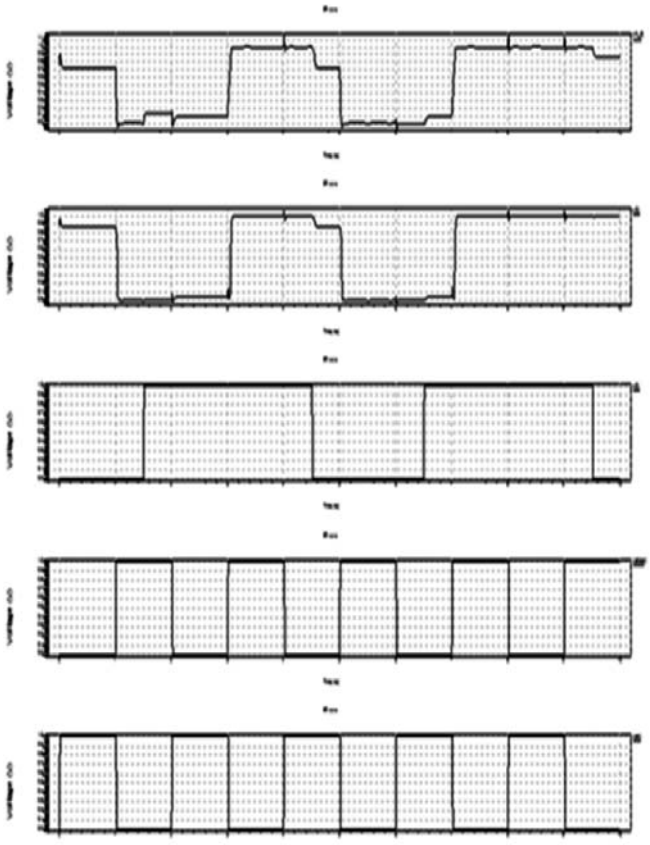

Fig. 5. Waveform of transient analysis of D FF for 90nm Technology

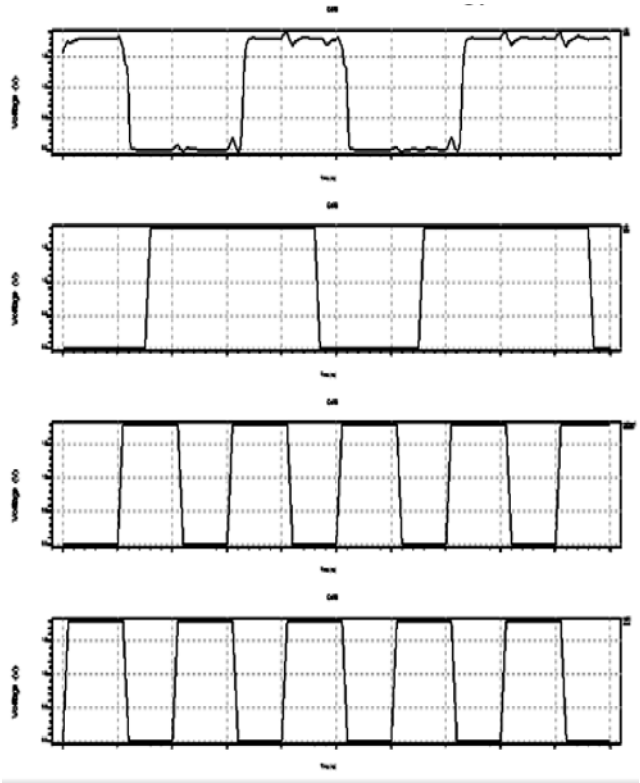

Fig. 6. Waveform of transient analysis of D FF for 180nm Technology

Average power consumed, maximum power, minimum power and delay at different technologies are given below. Comparison of various technologies in terms of power dissipation and delay is shown in the Table 2 and represented in the form of graph in Fig. 7.

At 45nm:

Average power consumed:
9.626436e-006 watts
Max power :
1.403208e-004 at time 7.015e-009
Min power :
4.335790e-008 at time 2e-009
Delay time : 1.8151e-009

At 90nm:

Average power consumed :
1.349961e-004 watts
Max power :
1.028858e-003 at time 7.04437e-009
Min power :
2.213917e-006 at time 9.0882e-009
Delay time : 2.0403e-009

At 180nm:

Average power consumed :
1.371639e-004 watts
Max power :
1.441726e-003 at time 7.27123e-009
Min power:
2.034298e-007 at time 3e-009
Delay time : 2.1413e-009

Table 1: Comparison between three technologies in terms of Power and Delay

Technology	Average Power (Watts)	Delay (Sec)
45nm	9.626436e-006	1.8151e-009
90nm	1.349961e-004	2.0403e-009
180nm	1.371639e-004	2.1413e-009

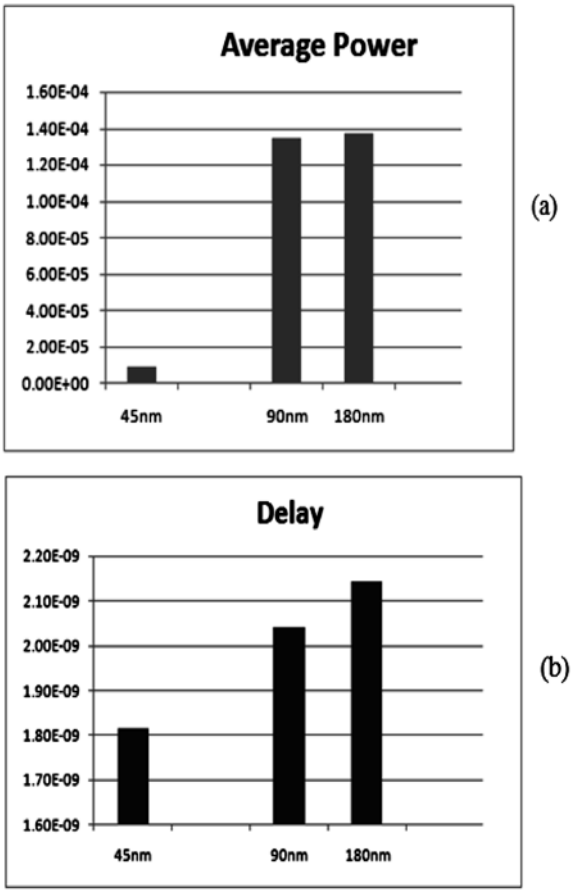

Fig. 7. Comparison of various technologies in terms of (a) Average Power and (b) Delay.

IV. CONCLUSION

From the simulation results it can be observed that design using 45nm technology has shown minimum delay and minimum power requirement which are the major requirement of low power applications. In the various digital circuit applications this flip flop is used as buffers, microprocessors, registers, digital VLSI clocking etc. Here the implemented design uses 8 transistors D flip-flop and performance of this D flip-flop has been calculated for various technologies. The performance of D Flip-Flop at 45nm has proven the best attainment in terms of area on the integrated circuit and dissipated power. Results of simulation represents that the delay is reducing by 92.86% and 1.58% when we shift towards 180nm to 90nm technology and 90nm to 45nm technology respectively. Correspondingly average power is decreased by 4.71% and 11.03% respectively with the shift in technology as given above.

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